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An Energy-Efficient Full-Adder Design Using Pass-Transistor Logic

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***Abstract*— Recently, the data processing capability of the electronic chip is increased significantly. In general data processing means the arithmetic operation on that data. As a result, we have seen that the ALU is present in any data processor. So, the full adder becomes an essential part of the logical and arithmetic unit of the processor. To improve the computational performance of the chip, the improvement of a full adder is necessary. An appropriate logic style helps the designer to design an efficient full adder. In this paper, several logic styles are briefly discussed. We choose to pass transistor logic style to design our new full adder. This logic style is used for reducing power consumption and increasing operational speed. The proposed adder consists of 10 transistors. LTSPICE simulator is used for simulating the schematic. 16nm low power high-k strained silicon transistor model is used for achieving design objectives. A practical transistor model is employed to encounter all practical aspects. The overall performance of the proposed adder circuit is analyzed and compared with conventional circuits.**

Keywords*— *ALU, Pass-Transistor Logic, Transmission Gate Logic, PTM model, Power-Delay Product.

I. INTRODUCTION

In order to keep the performance rate according to Moore's law is not possible only by improving the fabrication technology. We need to focus on other factors for improving the performance rate. A suitable circuit design is necessary for achieving this goal.

The microprocessor is a widely used VLSI circuit. The performance of the microprocessor is increasing day by day. Switching frequency & power consumption of a microprocessor has significantly improved over the past 10 years. ALU is the vital element of a microprocessor. The adder is one of the basic elements of ALU. Address calculator, Compressors, Code converter, etc. the most known VLSI application. ALU performs some arithmetic operation on the given data for example addition, subtraction, division, multiplication, logic analysis, etc. So, the primary building block of ALU is the full adder. It is necessary to improve the performance of the full adder because of improving the overall performance of the system.

An efficient adder design has also an impact on the performance of ALU, also microprocessor. The main goal in the design of VLSI circuits is to design high speed, low-power, full-swing output, full adders [6]. Now a day's designers try to reduce the power consumption of the VLSI circuit.

The major components of power consumption are switching power & short circuit power.

There are so many research papers that have been published based on full adder design using different logic styles. Maximum of them follow the basic Boolean equation of full adder and some of them use the modified Boolean equation of full adder. Conventional full adder based on CMOS logic gives full output swing but the power consumption and transistor count is very high. It has two networks known as pull-up and pull-down networks. Those are responsible for providing swing restoration. Other conventional full adders have existed which is based on CPL logic style. This adder has same characteristics as CMOS logic based full adder. These circuits need large amount of die area [5]. The signal degradation is the major problem of CPL based design.

Now the question arises how can we reduce the power consumption of adders and reduce the die size? The reduction of the number of transistors is the way to achieve compactness and low power consumption. So, we need to redesign where the goal is to design the circuit using as less transistor as possible. Pass Transistor Logic (PTL) is used to achieve low transistor count low power dissipation. Threshold voltage loss is the main drawback of PTL. So, it is useful to design any digital circuit using PTL where the impact of threshold voltage loss is less. In any Practical processor, there are so many arithmetic units, i.e. so many adder units [3]. For that reason, PTL logic is used in the proposed adder circuit. In this paper, we propose an adder circuit, which is a 10T adder and is based on PTL logic. 10T adders are also presented in some papers but the proposed adder has different Schematic from others as well as we use a practical transistor (MOSFET), model. The transistor model is taken from the PTM website. 16nm Low Power high-k strained silicon model [10] is used for the simulation of our adder circuits to measure some parameters. Strained silicon [8] is a layer that is epitaxially grown on the gate of a MOSFET to improve the transistor's mobility. We compare our findings with some existing adder circuits. In the next section, we will discuss some logic styles and some previous works on a full adder.

II. DIFFERENT LOGIC STYLES

If we want to design any digital circuit, we have to choose any logic styles. Digital circuit parameters such as its speed, size, power dissipation, etc. are influenced by its logic style. Propagation Delay depends on the number of transistors in the

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circuits, the geometry of the transistor and parasitic capacitance. So, choosing appropriate logic styles for designing any logical circuit is important for getting the optimum response of that circuit.

A. *Static and Dynamic Logic*

Static logic is a conventional logic style. In this logic style, the transistor's gate and VDD are connected directly to the ground through a low resistance path. On the other hand, the gate output depends on the clock or pulse from any temporary storage in dynamic logic. For a high-speed application, the dynamic logic gate is good but for low power applications, it is not suitable because it dissipates excessive power [4].

B. *Complementary CMOS Logic*

Complementary logic is a subclass of static logic. The upper and lower network is present in this logic style. The upper network consists of PMOS so it is called pull-up network and the lower network is consists of NMOS so it is called pull-down network. If the gate of the transistor of both networks in logic '0' the pull-up network is activated and the output will be high. If the gate of the transistor of both networks in logic '1' then-then the pull-down network is activated and the output will be low.

The layout of the CMOS is less complex and efficient due to complementary pairs but there is some drawback. In complementary CMOS logic, a large number of transistors is required as a result the area is increased. Another drawback of complementary CMOS is that it requires both NMOS and PMOS on each input [4].

C. *Pseudo NMOS Logic*

Pseudo NMOS logic is sometimes called the area efficient logic style. We know PMOS takes more area than NMOS. In pseudo NMOS logic, the entire PMOS network is replaced by one PMOS. Now if P is the number of PMOS in the upper network and Q is the number of NMOS in the lower network, in Complementary CMOS logic, P+Q transistor is needed (provided that P=Q) to implement P or Q input logic function whereas Q+1 transistor is needed for pseudo NMOS logic. V_{DD} is the high input voltage because the lower network is logically off when the output is high. GND is not the low voltage because the lower network is connected to the grounded PMOS load device. The PMOS and NMOS size ratio has a great role in the overall functionality of Pseudo NMOS. For that reason, this logic style is called the ratioed logic [4].

D. *DCVS Logic*

Differential logic and positive feedback are seen in this logic style. As a result, it removes static current and provides full output swing. The static current generates because of having a direct path between Vdd and Ground. The differential logic enables it to have its output, both in true in complementary form. The feedback mechanism ensures that the load device is turned off when not required. Due to cross-over currents, Power dissipation is still present. Both PMOS and pull-down networks are turned on for a short duration of time during the transition which provides a short circuit path. [4]

E. *CPL Logic*

In this logic, we get two outputs. One is normal and the second one is complemented. According to figure 1, two networks are there where one implementing the function F and the other network implementing F'. The logic structure is shown in figure 1.

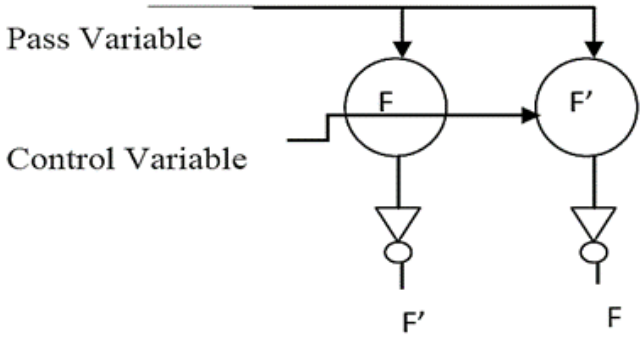

Figure 1: CPL logic structure [4]

Signal degradation is one of the major problems of CPL. This degradation occurs when the signal is going through many series-connected transistors. The degradation value is one threshold voltage.

F. *Double Pass-Transistor Logic*

In DPL, the true and complementary logic function is implemented by using both NMOS and PMOS. The Vth drop is eliminated which is seen in CPL [4].

G. *Transmission Gate Logic*

In Transmission gate logic, the drain and source of the NMOS and PMOS are connected and the gates are isolated. Here two types of control signals are needed. The original one is going to the gate of PMOS and its complement is going to the gate of NMOS. It has the ability to pass "TRUE and "FALSE". The combination of the characteristics of NMOS and PMOS gives this ability. The advantage of TG logic is to pass logic effectively without any distortion [4]. Figure 2 shows the logical structure of the TG logic.

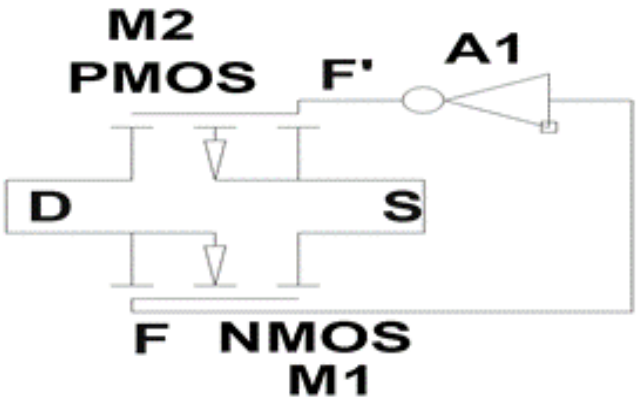

Figure 2: TG logic structure

III. DIFFERENT MODELS OF FULL ADDERS

A. *Conventional Full adder*

This full adder is based on CMOS logic style. The transistor count of this adder is 28 or somewhere 32. CMOS cells are used to design this adder. This adder has no threshold voltage loss and it gives the full swing of voltage but

consumes much power and propagation delay is significant. Figure 3 shows the conventional adder circuit [2].

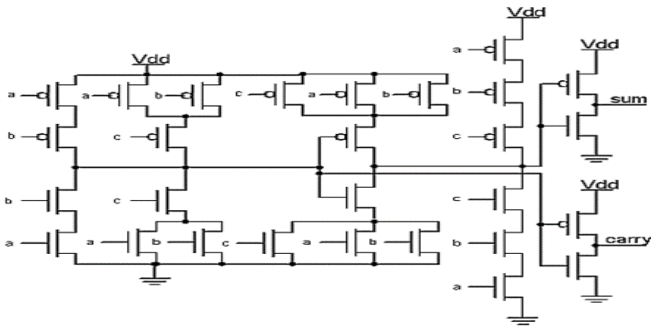

Figure 3: Conventional CMOS full adder

B. SERF Adder

SERF Adder means static Energy Recovery Full adder. In this adder, the charge which is drained during logic low is reused. It is used as an input signal to control the gates of the transistor. There is no direct path to ground. Hence the power dissipation due to short circuit current is completely reduced. Figure 4 shows the 10T SERF adder [3].

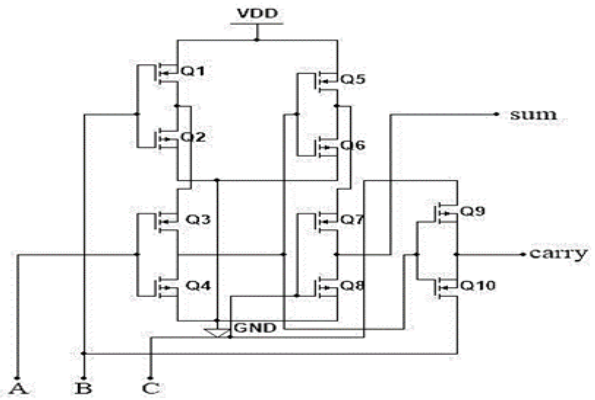

Figure 4: 10T SERF Adder

There is another kind of SERF adder commonly is called the 13A adder. Two types of XNOR are used in this type of adder. In terms of low power and delay, 13A adder performs much better than SERF adder. Figure 5 shows the schematic of the 13A adder.

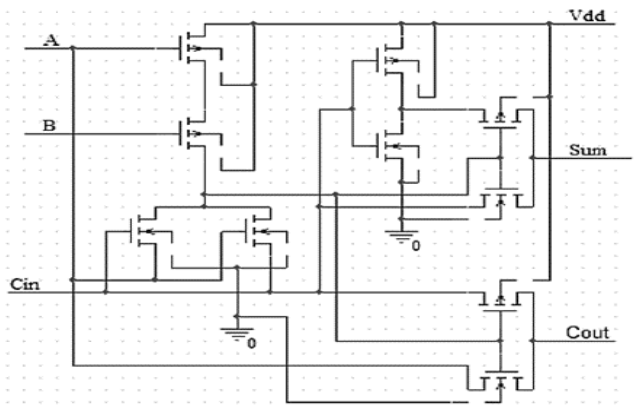

Figure 5: 13A Full Adder [3]

C. CLRCL Full Adder

One of the major disadvantages of PTL is its output is lost or reduced. As a result, we cannot get the full swing of output from the PTL based Circuit. In CLRCL adder three multiplexers and two inverters are used. One inverter act as a buffer which reducing the delay. Figure 6 shows CRLCL adder [3].

D. 6T Adder (Deepa, Sampath)

Deepa and Sampath [3] proposed the 6T adder in their paper. The base of this adder is MUX. Two transistors MUX is used in this adder. This 6T adder is applicable if all the input is available. That means there is no inverter for inverting any input and assumed that the inverted input is available. Figure 7 shows the schematic of the 6T adder proposed by Deepa and Sampath.

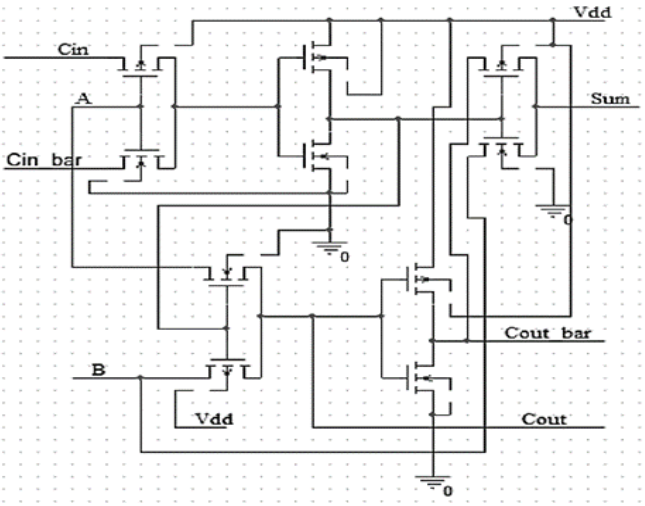

Figure 6: CRLCL Full Adder

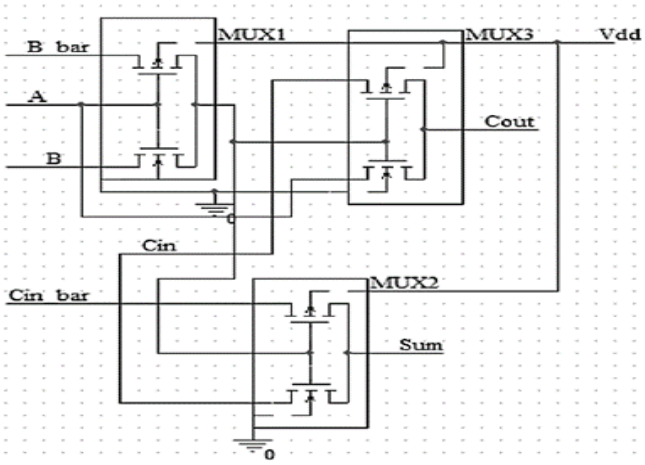

Figure 7: 6T full adder (Deepa, Sampath) [3]

IV. PROPOSED FULL ADDERS

So far, we have discussed the logic structure and previous works on the Full adder. There are some advantages and disadvantages of that adder which is discussed in the previous section. In this section, the new designed full adder circuit is discussed. PTL logic style is used to design our new full adder.

We also use the PTM Transistor model. In order to reduce the number of transistors, we use PTL logic. Our design goal is to reduce the area, reduce delay and high-speed operation. This circuit is designed using only 10 transistors. First, we precisely design the XOR unit and then design the full adder. The carry unit is designed using only 2 NMOS. Figure 8 shows the schematic of our new designed 10T full adder. The adder is designed using the following sum and carry equations

$$Sum = (A \oplus B) \oplus Cin \quad (1)$$

$$Carry = \{(A \oplus B) * Cin\} + (A * B) \quad (2)$$

The upper 8T (4 PMOS & 4 NMOS) generate sum and the lower 2 NMOS generate carry.

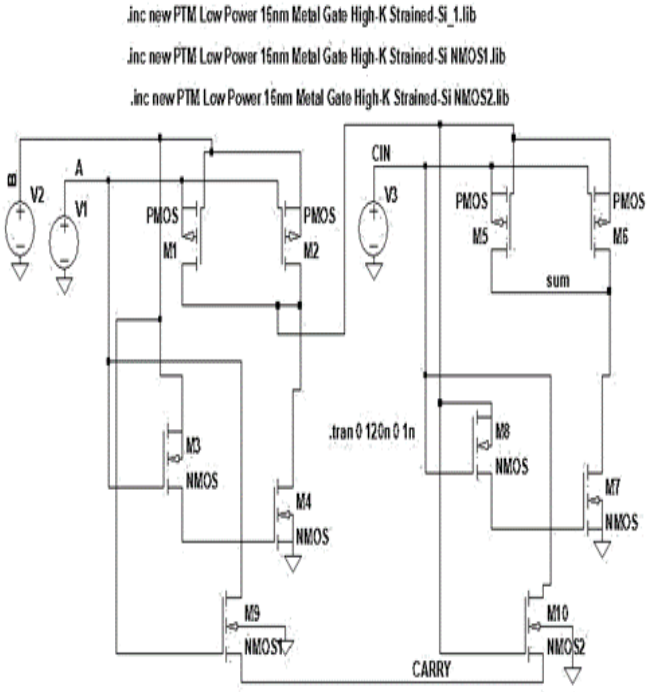

Figure 8: Proposed 10T Full Adder

Here, we explain how the schematic in figure 8 follow the equation 1 and 2. Refer to figure 8, the M1, M2, M3, and M4 transistors act as an XOR gate. Signal A and B are placed in the source of M1 and M2. We get the output A⊕B at the common drain of M1 and M2. Similarly, M5, M6, M7, and M8 transistors also act as an XOR gate. The output from the first XOR gate (A⊕B) and the signal C_{in} are placed in the source of M5 and M6. The output of the 2nd XOR gate (M5, M6, M7, M8) is A⊕B⊕C_{in}. we get that output at the common drain of M5 and M6. That is the sum of the adder which is written in equation 1.

Now the lower 2 transistors basically act as individual AND gate. The output from the 1st XOR gate is placed in the gate of the M10 transistor and signal C_{in} is placed in the drain of M10 transistor. So theoretically we get (A⊕B)*C_{in} at the source of M10. Similarly, signal A and B are placed in the drain and gate respectively of the M9 transistor. Then we get (A*B) at the source of M9. As the source of M9 and M10 are connected (Figure 1) according to TG logic we get {(A ⊕B)*C_{in} +(A*B)} at the common source of M9 and M10. That is the carry of the adder which is written in equation 2.

V. SIMULATION RESULT

We simulate the proposed adder circuit (figure 8) in order to measure some circuit parameters that evaluate the overall performance of the design. LTSPICE simulator is used for simulating our circuits. The simulation is carried out using a 16nm PTM model [10] with a power supply of 0.9v at frequency 25MHz. The input signals are shown in figure 9 and the output response of two proposed adders is shown in figure 10 [9] (only the first 3 cycles are shown)

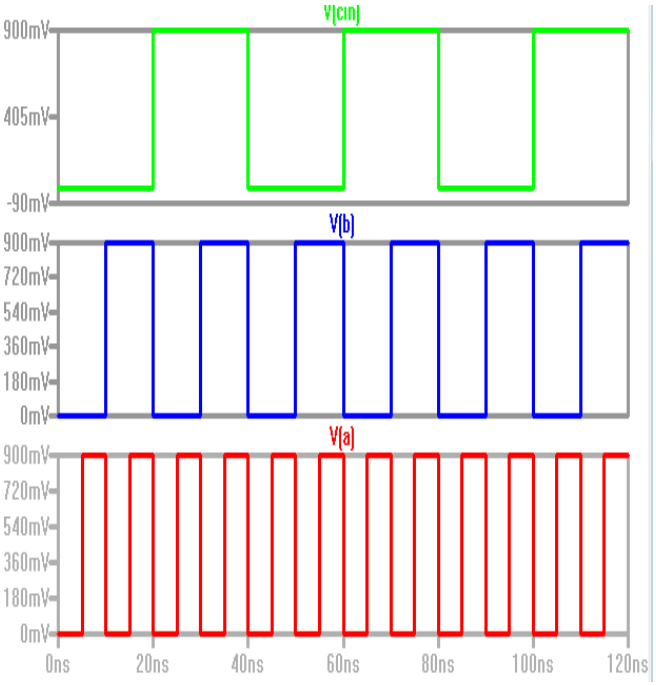

Figure 9: Input Signals (Cin, B, and A)

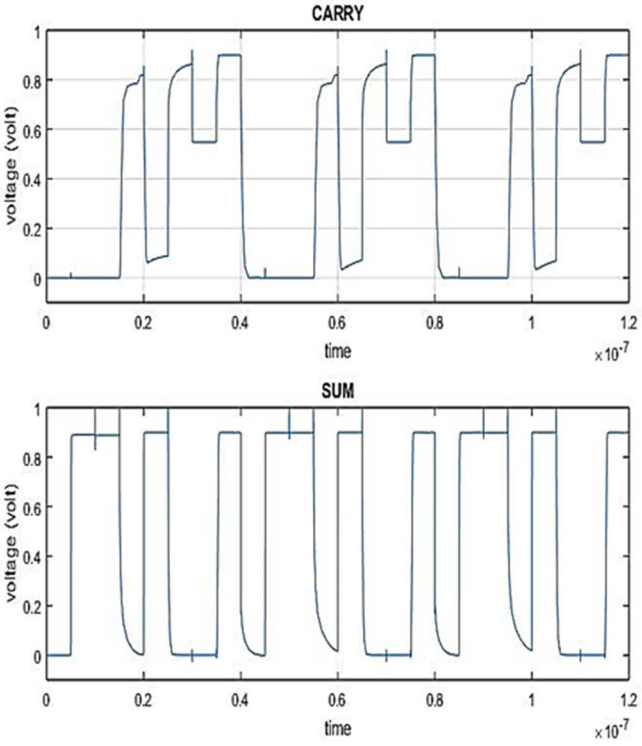

Figure 10: Output Response of 10T Adder

We compare the adder circuit with Deepa, Sampath 6T adder [3] and Reddy, Kavita 6T adder [2]. A comparison table of the measured parameters is given in Table I.

TABLE I. PERFORMANCE COMPARISON OF ALL ADDERS

List of ull Adders	*Average power (nW)*	*Average delay (carry) (s)*	*Average delay (sum) (s)*	*Total average delay (s)*	*PDP (nW. s)*
Proposed 10T adder	1.21	2.3e-10	8.0e-11	1.5e-10	1.9e-19
Deepa, Sampath adder [3]	3.56	1.2e-10	1.4e-10	1.3e-10	4.7e-19
Reddy, Kavita adder [2]	4.28	6.9e-11	8.6e-11	7.7e-11	3.3e-19

The bar graph is also added for a better understanding. The comparison of power, total delay, and PDP of all adders are presented in the bar diagram in Figure 11, Figure 12 and Figure 13.

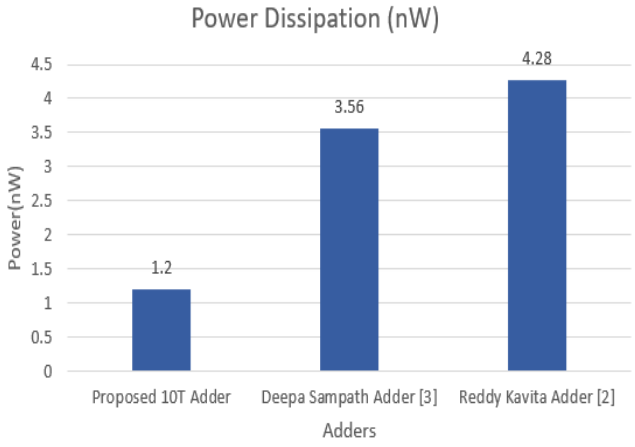

Figure 11: Power Consumption of all adders

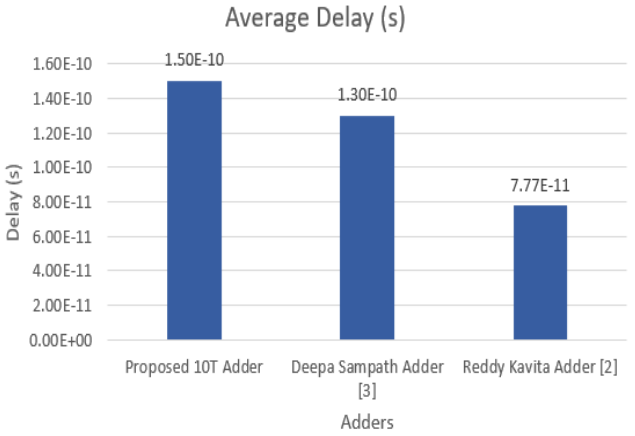

Figure 12: Total Average Delay of all adders

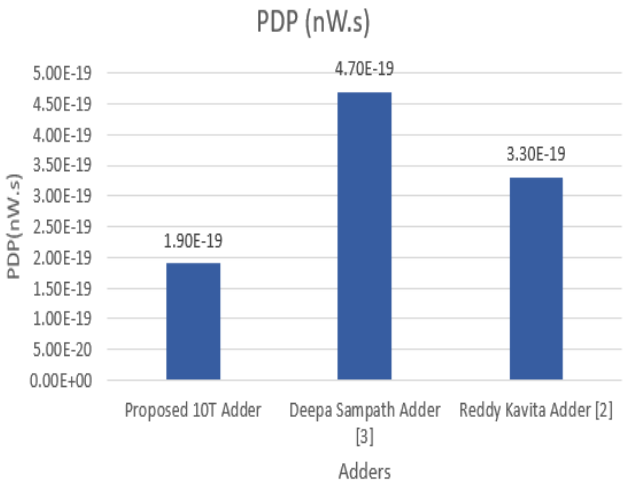

Figure 13: PDP of all adders

VI. CONCLUSION

An efficient adder cell/circuit is designed for improving the overall performance of other electronic circuits. This model is simulated extensively considering all practical aspects. LTSPICE tool is used for simulation. 16nm low power high k strained silicon transistor model is used to get nearly practical data. The basic parameters of the proposed circuit are calculated and compared to another existing adder circuit. In terms of compactness and power efficiency, the proposed adder is superior to conventional models, but the total average delay of proposed circuits is slightly higher. However, the proposed circuit has lower PDP than others. We can further improve our proposed circuit by using the FINFET or CNTFET model instead of a MOSFET model.

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