# Self-biased nano-power four-transistor current and voltage reference with a single resistor

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A generic nano-power voltage and current reference topology, which takes advantage of the unequal threshold voltage ($V_{TH}$) of two MOSFETs in subthreshold region, is developed to provide reliable bias and reference signals for the analogue integrated blocks used in the Internet-of-Things applications. The new architecture is a self-powered four-transistor topology with a single temperature-insensitive resistor, generating both temperature-independent voltage and current without any operational amplifier or bias network. Instead, the resistor defines the absolute value of the current reference ($I_{REF}$) which supplies the core devices. The circuit is designed and simulated for a target current reference of 7.50 nA in 0.18 μm CMOS process, and achieves a worst-case temperature coefficient (TC) of 59.47 ppm/°C over a temperature range from −40 to 125°C and 1.8 V voltage supply. The average voltage reference ($V_{REF}$) is 346 mV, and the worst-case TC of different corners is 21.98 ppm/°C. The nominal current consumption is twice the $I_{REF}$ (15 nA) regardless of the supply and temperature, and can be scaled down by reducing the desired current reference.

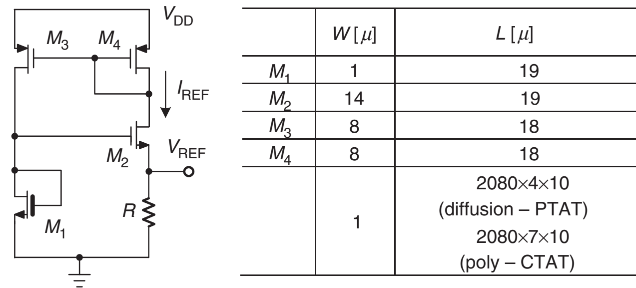
*Introduction:* Voltage and current references operating at nano-watt power level are highly demanded for battery-powered Internet-of-Things systems where the static power budget is extremely limited [1–3]. These circuits are, conventionally, realised using the MOSFETs biased in subthreshold regime. Many references are not, however, able to maintain a small temperature coefficient (TC) over a broad range of positive and negative temperatures [4] or generate voltage and current simultaneously. More important for our discussion, none of the self-biased two- and three-transistor references reported recently in [1–2, 4] can produce a temperature-insensitive current in their original architecture. Instead, the biasing current generated internally to power-up the circuit is proportional to $\mu V_T^2$ ($\mu$ is the carrier mobility, $V_T = kT/q$ is the thermal voltage, $k$ is the Boltzmann constant, $T$ is the absolute temperature, and $q$ is the electron charge), causing the dissipating power to rise by one or two orders of magnitude at high temperatures despite the optimal operation at room temperature. The configuration proposed in [3] can generate both $V_{REF}$ and $I_{REF}$. The implementation is, however, based on operational amplifier (opamp), adding multiple design constraints in terms of DC gain, noise, power, matching between the differential elements, bias network, stability, and frequency compensation. Besides these limitations, the opamp's input-referred offset voltage is temperature dependent, impairing the operation of the reference core in minimising the TC of the generated $V_{REF}$ and $I_{REF}$. In this Letter, we introduce a simple voltage and current reference in which most of the above-stated shortcomings are solved.

*Circuit configuration and analysis:* Fig. 1 shows the proposed self-regulating voltage and current reference. The MOS devices used in the schematic are all biased in subthreshold region to ensure low-power operation with minimum supply voltage. The voltage reference is equal to the gate-source voltage ($V_{GS}$) difference of the standard device $M_2$ and the I/O device $M_1$ which has a greater $V_{TH}$ due to increased gate-oxide thickness. The voltage $V_{REF}$ is loaded by the resistor $R$, producing a temperature-insensitive $I_{REF} = V_{REF}/R$ by forcing both $V_{REF}$ and $R$ to be independent of temperature. The devices $M_3$ and $M_4$ form a $p$MOS current mirror that makes the topology a self-powered configuration, also shield the sensitive core from the variations of unregulated voltage supply ($V_{DD}$). Denoting $W$ and $L$ as transistor's gate width and length, the current mirror conveys a $(W/L)_3/(W/L)_4$ ratio of $I_{REF}$ into the left branch and supplies $M_1$ by the same current. An analytical expression for $V_{REF}$ can be derived based on the $I$–$V$ characteristic of a $n$MOS operating in subthreshold area [4]

$$I = \mu C_{OX}(N-1)V_T^2\left(\frac{W}{L}\right)\exp\left(\frac{V_{GS}-V_{TH}}{NV_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right], \tag{1}$$

where $I$ is the subthreshold current, $V_{DS}$ is the drain-source voltage, $C_{OX}$ is the gate-oxide capacitance, and $N$ is the subthreshold slope factor. By neglecting the dependence of $I$ on $V_{DS}$, which is dominant only for the voltages below roughly $4 \times V_T$, and by assuming that $N_1 = N_2 = N$, the voltage reference can be computed by

$$V_{REF} = V_{GS1} - V_{GS2}$$
$$= V_{TH1} - V_{TH2} + NV_T \ln\left[\frac{(W/L)_2}{(W/L)_1}\cdot\frac{(W/L)_4}{(W/L)_3}\cdot\frac{\mu_2 C_{OX2}}{\mu_1 C_{OX1}}\right]. \tag{2}$$




| | $W [\mu]$ | $L [\mu]$ |
|---|---|---|
| $M_1$ | 1 | 19 |
| $M_2$ | 14 | 19 |
| $M_3$ | 8 | 18 |
| $M_4$ | 8 | 18 |
| | 1 | 2080×4×10 (diffusion – PTAT) 2080×7×10 (poly – CTAT) |

**Fig. 1** *Circuit diagram of the proposed voltage and current reference*

The threshold voltages $V_{TH1}$ and $V_{TH2}$ of $M_1$ and $M_2$ are both complementary-to-absolute-temperature (CTAT), and can be characterised using the following linear expression [1–4]:

$$V_{TH}(T) = V_{TH}((T_0) - \alpha(T - T_0), \tag{3}$$

where $V_{TH}(T_0)$ is the threshold voltage at the reference temperature $T_0$ where the slope factor $\alpha$ has been calculated. The coefficient $\alpha_1$ of $M_1$ is larger than $\alpha_2$ of $M_2$. The TC of $V_{TH1} - V_{TH2}$ is therefore negative and can be compensated by the opposite coefficient of the term related to $V_T$. A zero temperature coefficient $V_{REF}$ is achieved when

$$\frac{\partial}{\partial T}V_{REF} = \alpha_2 - \alpha_1 + \frac{Nk}{q}\ln\left[\frac{(W/L)_2}{(W/L)_1}\cdot\frac{(W/L)_4}{(W/L)_3}\cdot\frac{\mu_2 C_{OX2}}{\mu_1 C_{OX1}}\right] = 0. \tag{4}$$

Setting $(W/L)_3 = (W/L)_4$, an optimal relation between the aspect ratios of $M_1$ and $M_2$ is then obtained

$$\frac{(W/L)_2}{(W/L)_1} = \frac{\mu_2 C_{OX2}}{\mu_1 C_{OX1}}\exp\left[\frac{q}{Nk}(\alpha_1 - \alpha_2)\right]. \tag{5}$$

Replacing (5) into (2) results in a fixed ZTC $V_{REF}$ which is a function of the differences between the threshold voltages and the slope factors

$$V_{REF} = V_{TH1}(T_0) - V_{TH2}(T_0) + (\alpha_1 - \alpha_2)T_0. \tag{6}$$

The general $V_{REF}$ expression given by (2) depends only on the devices' aspect ratios and the physical properties of the $n$MOS devices (threshold voltages, gate capacitors, and carrier mobilities). The temperature characteristic of the biasing current will not therefore contribute to $V_{REF}$ as long as the branch currents are related by a fixed ratio. Nonetheless, the current $I_{REF}$ can be made insensitive to temperature when the resistor is also independent of temperature. Such a resistor may be realised by connecting a proportional-to-absolute-temperature (PTAT) and a CTAT resistor in series ($R = R_{PTAT} + R_{CTAT}$). Few choices with different temperature behaviour are available in CMOS technology, including poly, diffusion, and NWELL resistors.

*Case study:* A prototype of the proposed reference is simulated in 0.18 μm CMOS process. Fig. 1 presents the required element values for a target $I_{REF}$ of 7.5 nA when $V_{REF} = 346$ mV. The resistor $R$ is made by the series combination of a CTAT poly-resistor and a PTAT diffusion resistor. Choosing an aspect ratio of $W/L = 1\mu/10\mu$ yields a TC of −3.39 and +1.93 Ω/°C for the unit CTAT and PTAT resistors ($R_{U,C}$ and $R_{U,P}$), respectively. Fig. 2*a* shows the resulted 22.26 kΩ unit resistor ($R_U$) with TC = 53 ppm/°C over a temperature range of −40 to 125°C, when four $R_{U,C}$ and seven $R_{U,P}$ are connected in series ($R_U = 4R_{U,C} + 7R_{U,P}$). The resistor required to convert the 346 mV voltage reference into a 7.5 nA current reference would be therefore $2080 \times R_U$. Fig. 2*b* shows the layout of the proposed reference. The silicon footprint will be about 40% smaller if the diffusion resistors are replaced by kind of the NWELL resistors available in the same technology. The TC of $R$ would be, however, 137 ppm/°C instead of 53 ppm/°C. Further reduction of the resistor's area depends on the presence of high-resistive elements with linear TC in a CMOS technology. The TC of $I_{REF} = V_{REF}/R$ will be reduced if both $V_{REF}$ and $R$ follow the same temperature variations since

$$\frac{1}{I_{REF}}\cdot\left(\frac{\partial}{\partial T}I_{REF}\right) = \frac{1}{V_{REF}}\cdot\left(\frac{\partial}{\partial T}V_{REF}\right) - \frac{1}{R}\cdot\left(\frac{\partial}{\partial T}R\right). \tag{7}$$



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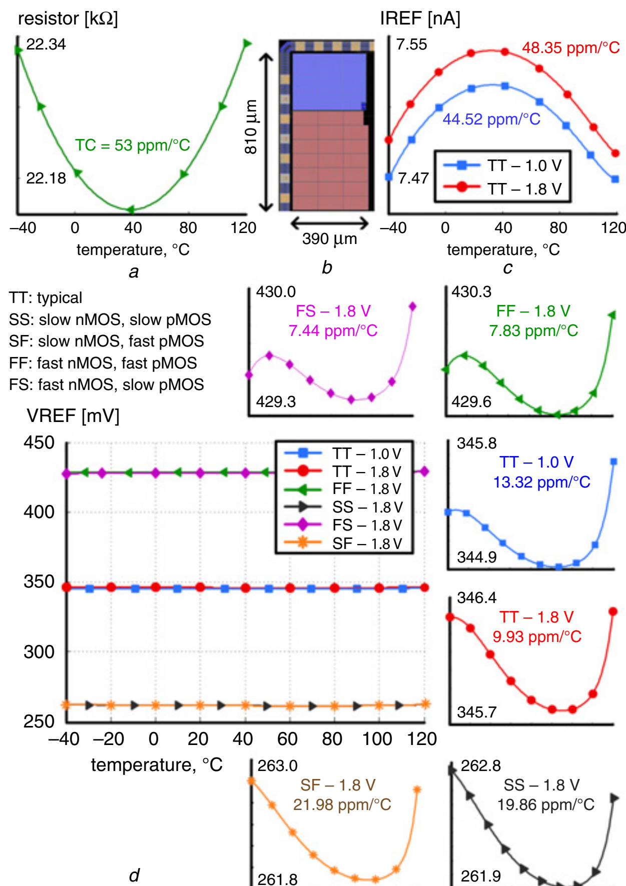


**Fig. 2** *Variations of different parameters versus temperature in the layout*

*a* Temperature-compensated unit resistor
*b* Details of the layout
*c* Current reference against temperature
*d* Voltage reference versus temperature at different process corners

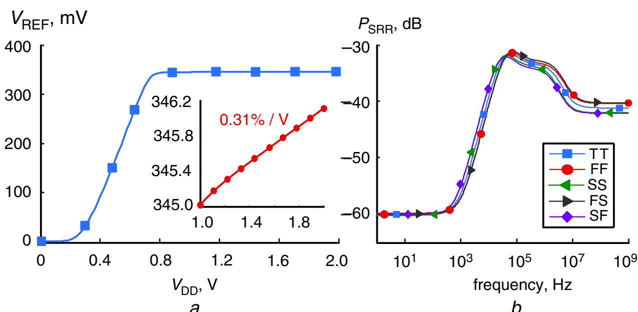


**Fig. 3** *Effect of voltage supply on the generated voltage reference*

*a* Supply dependence of $V_{REF}$ for the supply voltage range of 0–2 V
*b* PSRR versus frequency at room temperature ($V_{DD} = 1.8$ V)

In practice, however, the TC of $V_{REF}$ can be hardly compensated by the TC of $R$, and the resulted $I_{REF}$ has a higher TC compared to $V_{REF}$. Fig. 2*c* illustrates the simulated $I_{REF}$ versus temperature. The average TC of $I_{REF}$ is 48.35 ppm/°C for 1.8 V supply. Fig. 2*d* presents the temperature behaviour of $V_{REF}$ over the six process and $V_{DD}$ corners specified in each graph. An average TC of 9.93 ppm/°C is observed for the nominal case with $V_{DD} = 1.8$ V. The TC rises to 13.32 ppm/°C when the supply is dropped to 1.0 V. Without any trimming, the worst-case TC of $I_{REF}$ and $V_{REF}$ are 59.47 and 21.98 ppm/°C at the SF corner, respectively. Nonetheless, the absolute value of $I_{REF}$ can be easily tuned by trimming $R$ to account for the process variability. Fig. 3*a* shows the variations of $V_{REF}$ when $V_{DD}$ is increased from 0 to 2 V. The output voltage reaches its nominal value with <1% error for a line voltage of 0.8 V. The line sensitivity (LS) of $V_{REF}$ is 0.31%/V for the supply voltages beyond 1 V. The simulation result of the power supply rejection ratio (PSRR) versus frequency is plotted in Fig. 3*b*. The PSRR of $V_{REF}$ is −60 dB at 10 Hz, and remains below −33 dB despite no output capacitor being used to improve this parameter. Fig. 4 reports the Monte-Carlo simulation of $V_{REF}$ and its TC for 1000 iterations. The mean value ($\mu$) of $V_{REF}$ is 345.9 mV with a standard deviation ($\sigma$) of 0.61 mV, showing a variation coefficient of $\sigma/\mu = 0.17\%$. Table 1 compares the performance metrics with the other implementations reported in the prior art. The primary advantages of the new configuration are its capability to generate both $V_{REF}$ and $I_{REF}$ with small TC, ease of design and implementation, and nano-watt power consumption that is independent of temperature. The overall current is 15 nA, and can be changed according to the trade-off between power and the silicon area for on-chip integration of $R$.

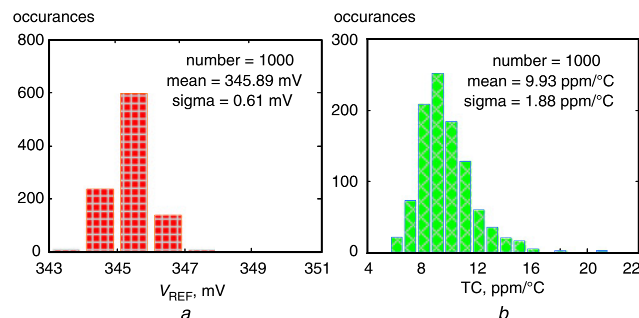


**Fig. 4** *1000-run Monte-Carlo simulation of* $V_{REF}$ *and its TC at 27°C*

**Table 1:** Performance summary and comparison

| | This work | [1][a] | [2] | [3] |
|---|---|---|---|---|
| type of ref. output | *I–V* | *V* | *V* | *I–V* |
| complexity | low | low | low | high |
| supply (V) | 0.8–2.0 | 0.4–1.2 | 0.4–1.8 | 0.7–2.0 |
| $V_{REF}$ (mV) – $I_{REF}$ (nA) | 346–7.5 | 27.2 | 151 | 368–9.97 |
| power (nW) | 12 | 0.05 | 1 | 28 |
| power versus temp. | fixed | exp. | exp. | fixed |
| TC of $V_{REF}$ (ppm/°C) | 21.98 | 159 | 89.83 | 43.1 |
| TC of $I_{REF}$ (ppm/°C) | 59.47 | N/A | N/A | 149.8 |
| temp. range (°C) | –40∼125 | –25∼125 | –40∼125 | –40∼125 |
| LS (%/V) | 0.31 | 0.08 | 0.163 | 0.027 |
| PSRR (dB) @ Hz | –60@10 | –98@100 | –73@10 | –59@10 |

[a]Four-transistor implementation.

*Conclusion:* A self-powered nano-power voltage and current reference is proposed based on four transistors and a single resistor. Simulation results show a worst-case TC of 21.98 and 59.47 ppm/°C for the voltage and current, respectively, while the power is made independent of supply and temperature. No opamp or bias network is used in the proposed topology, making it a good candidate to produce robust reference voltage and current for the analogue units in CMOS technology.

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One or more of the Figures in this Letter are available in colour online.

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