Design of High-Speed Low Variation Static Noise Margin Ternary S-RAM Cells

Yogesh Shrivastava and Tarun Kumar Gupta

***Abstract*—In this article, two ternary SRAMs are proposed with a lower delay than their predecessor. Both proposed SRAMs use an improved inverter, which is a fundamental building block of SRAMs. Due to this improvement, the speed of storing/retrieving data to/from the SRAM cells increased. The first proposed ternary SRAM cell uses different terminals for read and write operations to avoid the read disturb problem. The second proposed SRAM cell does not require an additional middle voltage (0.45V) to store ternary '1'. The first ternary SRAM cell requires a ternary sense amplifier to detect all the ternary level voltages, whereas the second ternary SRAM cell uses a simple two-level voltage detection sense amplifier. Further to observe the robustness of the proposed SRAM cells, Monte-Carlo analysis (process variation) was conducted over average power consumption, delay, power delay product (PDP), and static noise margin (SNM) by varying the diameter of the carbon nanotube and length of the channel.**

***Index Terms*—Terany logic, CNFET, SRAM, average power consumption, delay, PDP.**

I. Introduction

THE NUMBER of applications requiring memory cells is increasing nowadays. The requirement of memory cells with low power consumption and high capacity is rising in fast computing and communication systems. Ternary logic can fulfill this requirement in a simple and energy-efficient way. Digits in ternary logic are called trits; introducing an intermediate level in the ternary logic increases the memory cell's capacity. The ternary logic implemented using MOSFET (Metal Oxide Semiconductor Field Effect Transistor), either using transistors of different thresholds or varying the transistors' threshold voltage, by applying the appropriate voltage to the bulk terminal [1]–[4]; these are power-consuming and inefficient processes. Using CNFETs by exploiting their multi-threshold function makes them a better replacement to implement ternary logic [5]–[9]. Two ternary SRAM cells proposed in this article using CNFETs multi-threshold function by varying their chirality.

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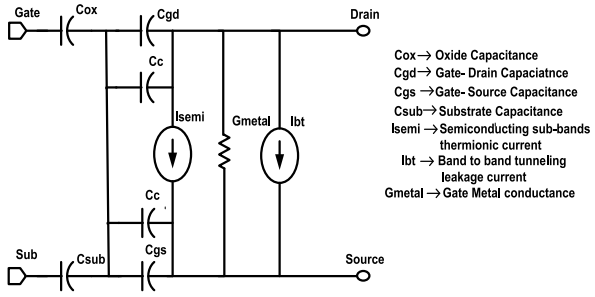

Fig. 1. Equivalent circuit model of CNFET.

A. CNFET

The CNFET assembly has a Single-Walled CNT (SWCNT), which contains only one cylinder. The equivalent circuit model of the CNFET is shown in Fig. 1 [10], [11], [24]. The angle of atom arrangement along the tube is called the chirality vector, represented by the pair (n, m). If $n = m$ or $n - m = 3i$ (i is an integer), then the CNT acts as a conductor otherwise as a semiconductor. The diameter of CNFET (D_{CNT}) has given in Eq. (1), where $a_0 = 0.142nm$ is the interatomic distance between 2 carbon atoms [4]–[9].

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{(n^2 + m^2 + nm)} \tag{1}$$

Based on the chiral vector CNFET is classified into three types, such as, armchair, zigzag and chiral; for armchair type, chirality is (n, n), which means $n = m$, in zigzag type, chirality is $(n, 0)$; for chiral type, chirality is (n, m). In the proposed and existing SRAM designs, the zigzag type of CNFET with semiconductor property is required and utilized [12], [13].

I-V characteristics of CNFET is similar to MOSFET. The threshold voltage (v_{th}), is the voltage required to turn ON the transistor, can be calculated as follows [14], [15], [25]

$$v_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV\pi}{eD_{CNT}} \tag{2}$$

Here, a = 2.49Å is the carbon to carbon distance, $V\pi$ = 3.033eV is the carbon $\pi - \pi$ bond energy in the tight bonding model, e is the unit electron charge. Effect of varying D_{CNT} on v_{th} is given explicitly in Table I. Table I concludes that the D_{CNT} and v_{th} are inversely proportional [13], [14].

In this article, CNFET with chirality (19, 0), (13, 0) and (10, 0) with D_{CNT} 1.487nm, 1.018nm and 0.783nm respectively, are used [18]–[20]. All the ternary circuit designs proposed in this article using the CNFET technology. The

TABLE I
CHIRALITY, D_{CNT} WITH THEIR CORRESPONDING v_{th} FOR P-CNFET AND N-CNFET

Chirality(n, m)	D_{CNT} (nm)	v_{th} (P-CNFET)	v_{th} (P-CNFET)
5,0	0.39	-1.10V	1.10V
6,0	0.47	-0.92V	0.92V
7,0	0.55	-0.79V	0.79V
8,0	0.63	-0.69V	0.69V
9,0	0.70	-0.61V	0.61V
10,0	0.78	-0.55V	0.55V
11,0	0.86	-0.50V	0.5V
12,0	0.94	-0.46V	0.46V
13,0	1.02	-0.42V	0.42V
14,0	1.10	-0.39V	0.39V
15,0	1.17	-0.37V	0.37V
16,0	1.25	-0.34V	0.34V
17,0	1.33	-0.32V	0.32V
18,0	1.41	-0.31V	0.31V
19,0	1.49	-0.29V	0.29V
20,0	1.57	-0.27V	0.27V

TABLE II
DEVICE PARAMETERS OF CNFET

Parameters	P-CNFET/N-CNFET
Supply voltage (Vdd)	0.9V
C-C atom distance (ring size)	0.2495nm
C-C bond length	0.141nm
Chiral indices (n,m)	(19, 0)
Radius of CNT	0.754nm
Thickness of oxide	4.754nm
Channel (nanotube) length (Lmin)	32nm
Dielectric constant of gate oxide	16

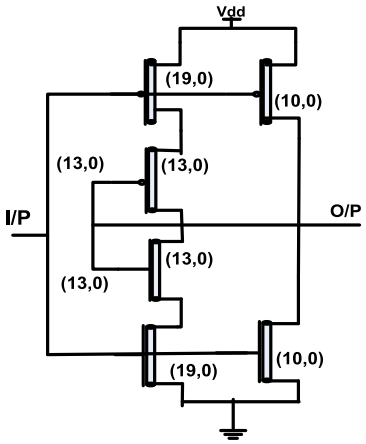

Fig. 2. Static ternary inverter proposed in [17].

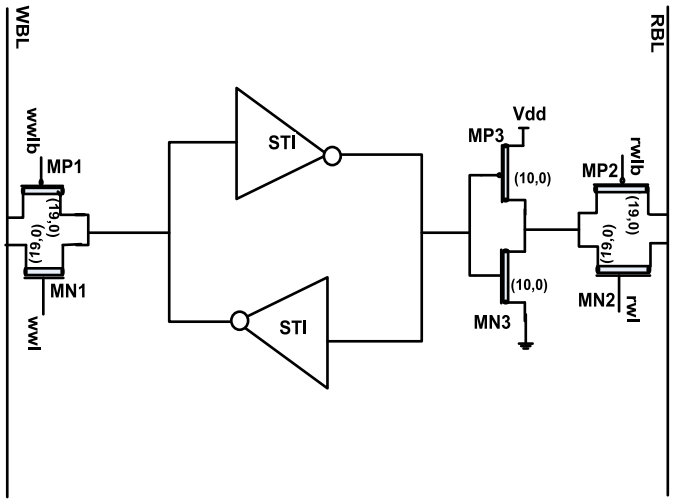

Fig. 3. SRAM cell proposed in [18] (TSRAM 1).

CNFET's Stanford University 32nm model file is used with the HSPICE simulator for simulation and obtaining the results [11]–[12]. The device parameters of CNFET are given in Table II [10].

The structure of this article is as follows. The Existing ternary memory cells are discussed in the following section. Proposed ternary memory cells are discussed in Section III. The simulation results of the proposed memory cells are summarised in Section IV. Finally, the conclusions drawn are illustrated in Section V.

II. REVIEW LITERATURE

The static ternary inverter (STI) proposed in [17], shown in Fig. 2, were used in the SRAM cell proposed in [18], shown in Fig. 3. The SRAM cell used a single-ended mechanism for read and write operations. The data forced on the Write Bit Line (WBL) to write into the memory cell through the write transmission gates (MN1 and MP1). The read buffer consists of transistors P-CNFET and N-CNFET, MP3, and MN3, respectively, with chirality (10, 0) and transmission gates (MN2 and MP2). The RBL was pre-charged to 0.45V, and according to stored-value, RBL was charged/discharged to 0.9V/0V or remained at 0.45V. This type of SRAM cell required a sense amplifier that can detect 0V, 0.45V, and 0.9V. This SRAM cell refers to TSRAM 1 in this manuscript.

Due to the single-ended functionality of TSRAM 1, the SNM improved with standby power consumption for '0' and '2' states, and the SRAM is free from the read disturb problem. The TSRAM 1 required a ternary sense amplifier, and the delay to write and read trit '1' is higher in this SRAM.

Two ternary CNFET SRAMs based standard ternary inverter of [17] was presented in [22], shown in Fig. 4 and 5. The chirality of the CNFETs was changed to improve the SNM and to reduce power dissipation in the 1st proposed SRAM of [22]. By increasing the chirality of CNFET used in the ternary SRAM, read and write delay reduced, and PDP improved. In the second proposed SRAM cell, two more transistors added, as shown in Fig. 5, to reduce the number of bit lines during the storage of trit '1'. The addition of transistors in the proposed 2nd SRAM of [22] caused a marginal increase in power consumption. The 2nd proposed SRAM of [22] refer as TSRAM 2 in this manuscript. Although The SRAMs proposed in [22] improved the delay of storing the trits over TSRAM 1, here

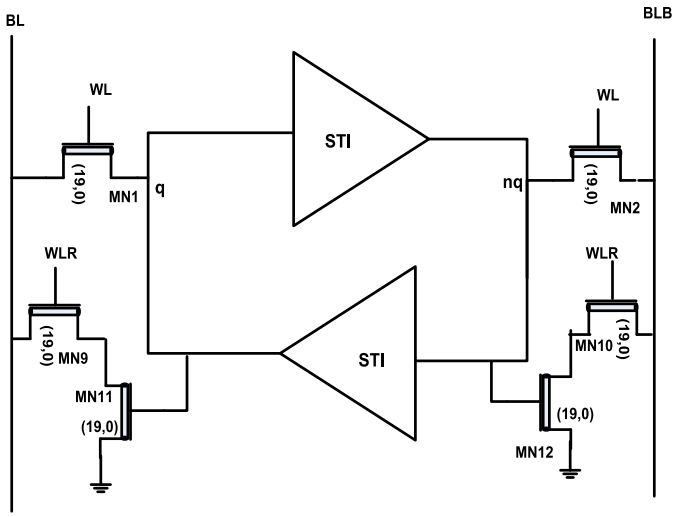

Fig. 4. 1^{st} SRAM cell proposed in [22].

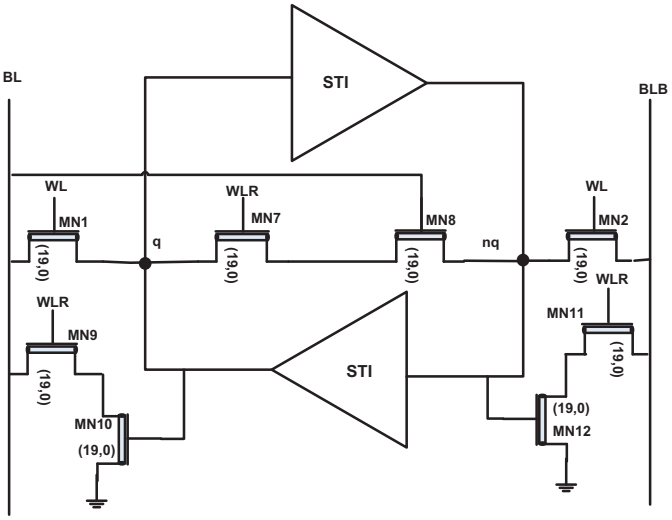

Fig. 5. 2^{nd} SRAM cell proposed in [22] (TSRAM 2).

in this article, an alternative method is proposed by which the delay is further reduces.

III. Proposed Ternary S-RAMs

A. Proposed Ternary SRAM 1

The traditional SRAM cells use back to back inverter to store the bit; additional pass transistors uses to read and write from memory cells. The ternary inverter proposed in [17] has two parts: one part contains four transistors, which activated when input '1' is applied, the second part contains only 2 transistors, and this part activated when the input is '2' or '0'. This arrangement provides delay while the input is 1, making the circuit's response sluggish [22]. To compensate problem, in existing STI, an additional diode pair is introduced in parallel with existing diode pairs, as shown in Fig. 6. The low delay ternary encoder circuit of [20] used the same concept. Herewith the same concept, the SRAM cell delay for input '1' reduces, and the memory cell's response becomes faster.

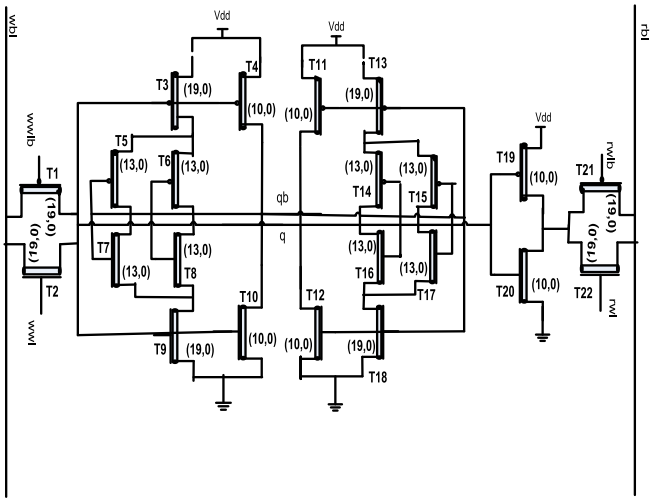

Fig. 6. Proposed ternary SRAM 1.

As shown in Fig. 6, there are two transmission gates in the proposed memory cell. One for the write operation (wbl) and the other one for read operation (rbl). When the voltage of the input pulse applied at 'wwlb,' and 'wwl' is greater than the threshold voltages of transistors T1 and T2, the voltage at 'wbl' transfers to the memory cell.

1) When the transferred voltage is ternary '0' transistor T4 becomes ON, the Vdd directly connects with node qb, and the voltage level at qb is ternary '2'. When the qb is at ternary '2', transistor T12 becomes ON, node q connects with the ground, and the voltage of node q becomes 0.
2) When the transferred voltage is ternary '2' transistor T10 becomes ON, the voltage of node qb becomes zero, at the same time transistor T11 becomes on and Vdd directly connects with node q and voltage of node q becomes high.
3) When the transferred voltage is ternary '1' transistors T3 and T9 become ON and transistors T5, T7 and T6, T8 provided parallel less resistive path for current to flow from Vdd to ground and voltage at node qb becomes ternary1. Similarly, T13 and T18 become ON, and transistors T14, T16, and T15, T17 provided parallel less resistive parallel path for current to flow from Vdd to ground and voltage at node q becomes '1'.

The read operation depends upon the transistors T19, T20, and transmission gates T21 and T22.

1) The rbl pre-charge with 0.45V. When the memory cell is holding ternary '0' transistor, T20 becomes ON, and rbl discharges.
2) When the memory cell is holding ternary '2' transistor, T19 becomes ON, and the pre-charged rbl further charges to vdd.
3) When the memory cell is holding ternary '1' , both the transistors T19 and T20 are OFF, and pre-charged rbl remains at 0.45V.

This circuit requires a sense amplifier circuit, which decides the exact level of the voltage at read output, whether 0, 1 or 2.

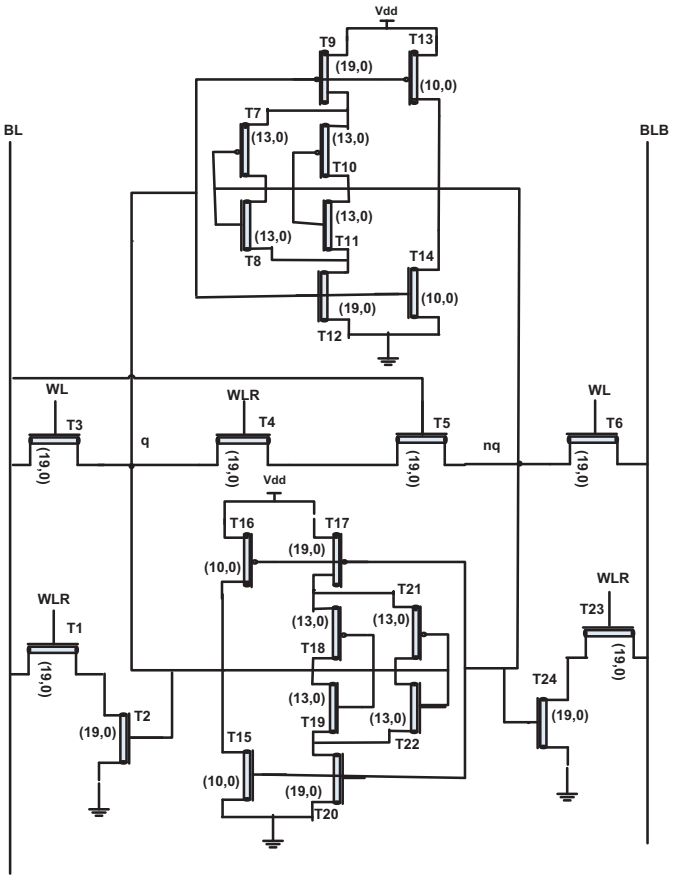

Fig. 7. Proposed Ternary SRAM 2.

B. Proposed Ternary S-RAM 2

The proposed S-RAM 2 is based on TSRAM 2, as shown in Fig. 7. In this S-RAM cell, there is no extra input of 0.45V (Ternary '1') is required, due to that such type of RAMs are closer to conventional binary RAMs: which have only 2 inputs, 0 (0V) and 1 (0.9V). In proposed SRAM 2 shown in Figure 7, when BL is 0V, BLB is 0.9V and the pulse voltage applied at the gate of transistors T3 and T6 is greater than the threshold voltage, the voltage of q is 0V (Ternary '0') and nq is 0.9V (Ternary '2'). In this way, ternary, '0' is stored in the memory cell.

When BL is 0.9V, BLB is 0V, and the pulse voltage applied at the gate of transistors T3 and T6 is greater than the threshold voltage, the voltage of q is 0.9V (Ternary '2') and nq is 0V (Ternary '2'). In this way, ternary '2' stores in the memory cell. When BL is 0.9V, BLB is 0V, WL is 0V and WLR is high, transistors T4 and T5 become ON. Both the inverters become parallel to each other and applied voltage divided into half and ternary '1' stores in the memory cell. There is no requirement for additional voltage other than 0V and 0.9V in this memory circuit. Due to transistors T7, T8, and T21, T22 low resistive path is provided for the current to flow from Vdd to ground.

For the read operation, the BL and BLB remained pre-charged to Vdd or discharged through the read buffers created by transistors T1, T2, and T23, T24 according to the stored values. The outputs are 0.9V and 0V, 0.9V and 0.9V, and 0V and 0.9V for stored ternary values 0, 1, and 2 respectively.

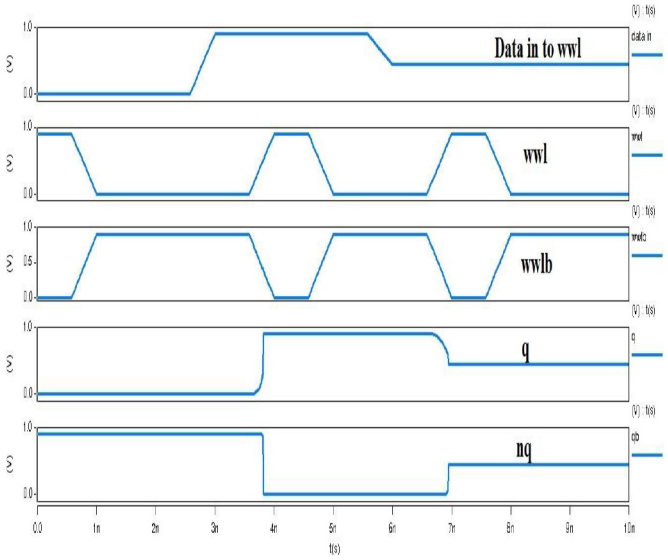

Fig. 8. Write operation of Proposed ternary SRAM 1.

This memory cell does not require the three-bit sense amplifier; instead, this cell is compatible with a conventional binary sense amplifier, similar to TSRAM 2.

IV. Simulation Results and Discussion

All the simulations have performed using the CNFET Stanford 32nm model [10], [11] using the HSPICE simulator. In this model, the default chirality of CNFET is (19, 0). The appropriate values of $n1$ and $n2$ (which represent the chirality vectors n and m, respectively) are selected to vary the chirality. Table I shows the default values of other parameters. The supply voltage is 0.9V. The proposed SRAMs are analyzed in a 1×128 memory structure to check the proper functioning. The following section discusses the write and read operations of standard and proposed SRAMs. The simulation environment is the same as opt by Lin *et al.* [18], Cho and Lombardi [22] followed the same simulation setup.

A. Write Operation

The power consumption, delay, and PDP (multiplication of average power consumption and delay) during the write operation of TSRAM 1, TSRAM2, Proposed SRAM 1 and Proposed SRAM 2 are shown in Table III, Table IV, Table V and Table VI respectively. The PDP is also related to the energy consumption of the cell. The write operation of the proposed ternary SRAM 1 and 2 are shown in Fig. 8 and 9, respectively. Fig. 8 verifies the working of proposed ternary SRAM 1, discussed in the previous section; with the first pulse input, the data stored in the proposed SRAM 1 is cleared; with the second pulse, ternary 2 stores in the SRAM and with third pulse input the stored data level shift to ternary 1. Fig. 9 verifies the working of proposed ternary SRAM 2, discussed in the previous section; with the first WL pulse input, the data stored in the proposed SRAM 1 is cleared, with the pulse input at WLR ternary 1 stores in the SRAM and with the third pulse input at WL the stored data level shifts to ternary 2 from 0.

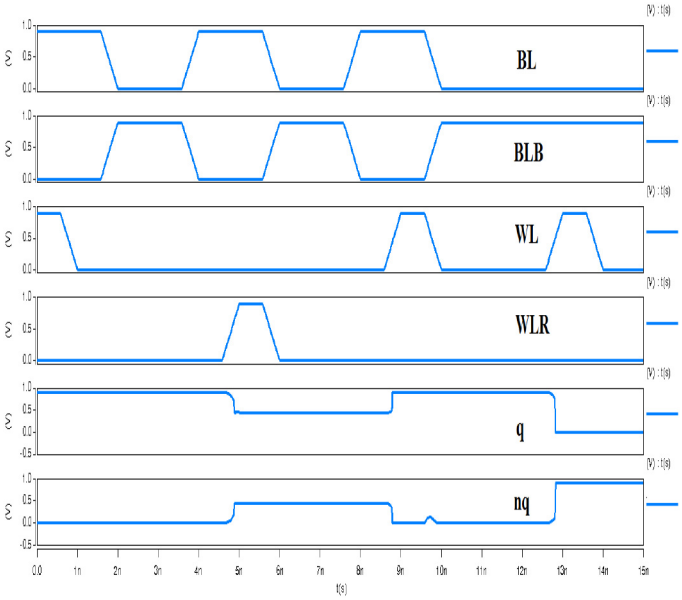

Fig. 9. Write operation of Proposed ternary SRAM 2.

TABLE III
WRITE OPERATION OF TSRAM1 [18]

Transition	Power Consumption (nW)	Delay (ps)	PDP (aJ)
0→1	359.28	134.27	48.2
0→2	89.25	51.421	4.5
1→2	370.98	190.76	70.8
1→0	1040.27	54.967	57.2
2→0	70.302	51.118	3.59
2→1	1007.45	258.03	260
Average	489.5887	123.427	74.1

TABLE IV
WRITE OPERATION OF TSRAM2 [22]

Transition	Power Consumption (nW)	Delay (ps)	PDP (aJ)
0→1 2→1	605.71	98.726	59.79
0→2 2→0	146.4	22.959	3.36
1→2 1→0	429.77	203.58	87.49
Average	393.96	108.42	50.21

The observation of Tables III, IV, V, and VI, concludes that the average power consumption is minimum in the TSRAM 2; it is 19.53% less than the TSRAM 1, 34.88% less than the proposed ternary SRAM 1, and 38.63% less than the proposed ternary SRAM 2. The minimum average delay observed in the proposed ternary SRAM 2 is 55.98% less than the TSRAM 1, 49.89% less than the TSRAM 2, and 25.49% less than the proposed ternary SRAM 1. The minimum average PDP observed in the proposed ternary SRAM 2 is 41.30% less than the TSRAM 1, 13.38% less than the TSRAM 2, and 15.55% less than the proposed ternary SRAM 1. The proposed ternary SRAM 2 provides less delay at the expense of power consumption, but the overall energy consumption is less among all the designs discussed above.

TABLE V
WRITE OPERATION OF PROPOSED TERNARY SRAM 1

Transition	Power Consumption (nW)	Delay (ps)	PDP (aJ)
0→1	537.41	114.4	61.5
0→2	91.332	22.173	2.03
1→2	584.34	107.98	77.208
1→0	1211.2	23.97	29
2→0	86.72	20.766	1.46
2→1	1119.2	148.23	165.89
Average	605.0337	72.91983	53.9

TABLE VI
WRITE OPERATION OF PROPOSED TERNARY SRAM 2

Transition	Power Consumption (nW)	Delay (ps)	PDP (aJ)
0→1 2→1	891.47	51.81	46.18
0→2 2→0	146.4	19.436	3.346
1→2 1→0	888.13	91.719	82.09
Average	642	54.321	43.872

TABLE VII
READ OPERATION OF TSRAM 1

Data (trit) stored	Power Consumption (nW)	Delay (ps)	PDP (aJ)
2	114.28	179.7	20.5
1	892.82	177.22	158
0	153.89	101.6	15.6
Average	386.9967	152.84	64.7

TABLE VIII
READ OPERATION OF TSRAM 2

Data (trit) stored	Power Consumption (nW)	Delay (ps)	PDP (aJ)
2	78.8	79.435	6.25
1	701.24	73.377	51.45
0	109.27	76.211	8.32
Average	296.4367	76.341	22

TABLE IX
READ OPERATION OF PROPOSED SRAM 1

Data (trit) stored	Power Consumption (nW)	Delay (ps)	PDP (aJ)
2	88.256	180.98	16
1	1245.5	101.33	125
0	180.19	94.71	12.7
Average	504.6487	125.6733	51.23333

B. Read Operation

The power consumption, delay, and PDP during the read operation of stored trit of the TSRAM1, TSRAM2, and proposed ternary SRAM 1 and proposed ternary SRAM 2 are given in Table VII, VIII, IX, and X, respectively. The read operation of proposed SRAM 1 and proposed SRAM 2 is shown in Figure 10 and 11, respectively. From Figure 11, it is clear that the proposed ternary SRAM 2 is compatible with binary sense amplifier.

The minimum average power consumption during the read operation observed in the TSRAM 2 is 23.4% less than the

TABLE X
READ OPERATION OF PROPOSED SRAM 2

Data (trit) stored	Power Consumption (nW)	Delay (ps)	PDP (aJ)
2	96.016	79.833	7.666
1	1121	47.257	52.975
0	68.811	76.26	5.24
Average	428.609	67.78333	21.96033

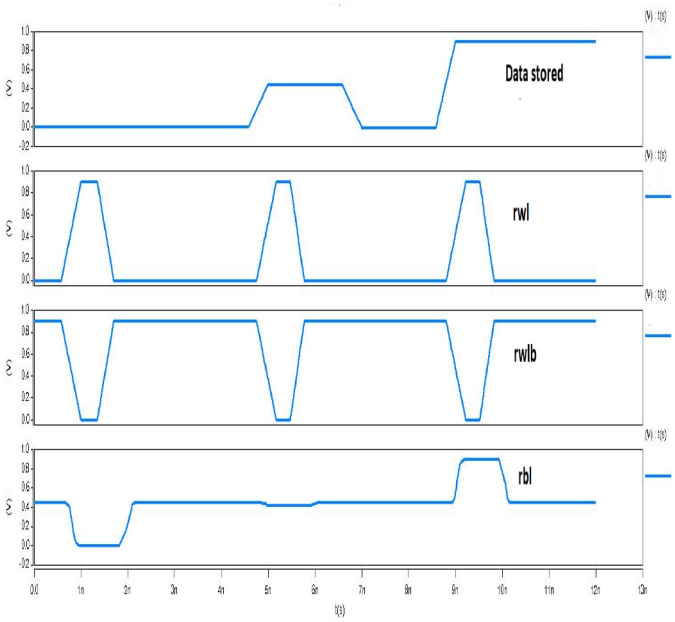

Fig. 10. Read operation of Proposed SRAM 1.

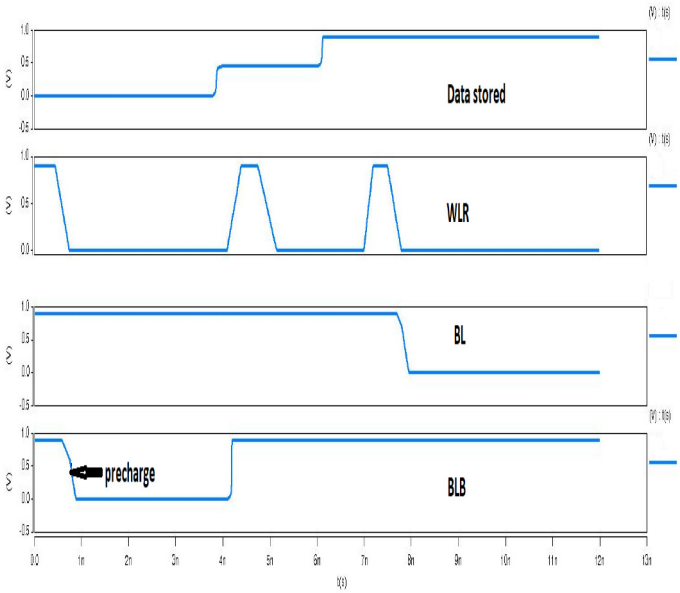

Fig. 11. Read operation of Proposed SRAM 2.

TSRAM 1, 41.25% less than the proposed ternary SRAM 1, 30.83% less than the proposed ternary SRAM 2. The minimum delay observed in the proposed ternary SRAM 2, which is 85.057% less than the TSRAM 1, 11.21% less than the TSRAM 2 design, and 46% less than the proposed ternary

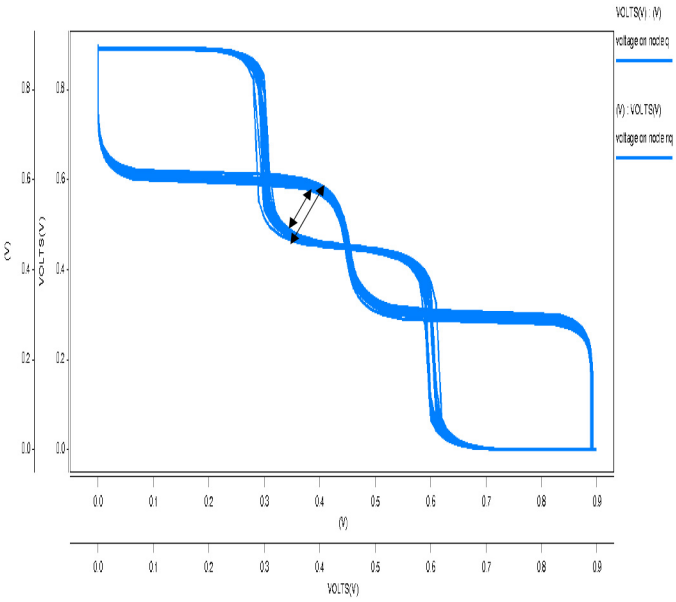

Fig. 12. VTC curve of proposed ternary SRAM 2.

SRAM 1. The PDP of the proposed ternary SRAM 2 and the TSRAM 2 is almost the same because the proposed design's average delay is minimum with the trade-off with power consumption.

C. Process Variations

The systematic and random variations in the process are among the significant challenges in designing nanoscale devices and circuits. It is problematic to obtain the exact size of the parameter; therefore, the process variations become a severe concern, negatively affecting the transistors' performance. In this section, the impact of process variations on parameters (power consumption, write delay, and PDP) over existing and proposed SRAM designs are discussed and evaluated. The deviations and mismatches in the diameter of the nanotubes D_{CNT} and the channel length L_{ch} of the carbon nanotube transistors have the most significant impacts on the performance of the CNFET-based circuits [23]. The Monte-Carlo transient analysis with a reasonable number of 30 samples for each simulation is conducted using the HSPICE simulator. The statistical significance of 30 samples is relatively high. If a circuit operates appropriately for all the 30 samples, there is a 99% probability that over 80% of all the possible component values operate correctly [23]. The distribution of the diameter and channel length is assumed as Gaussian with 6-sigma distribution, a reasonable supposition for large numbers of fabricated CNTs [19], [23].

The mean values of D_{CNT} and L_{ch} for the analysis is taken the same as given in Table II. The mean and standard deviation of the power consumption, delay, and PDP are observed. The values obtained from the Monte-Carlo analysis enlist in Table XI and Table XII for variation in D_{CNT} and L_{ch}, respectively.

The standard deviation is the measure of how much the samples deviate from the mean value. From Table XI, it can

TABLE XI
PROCESS VARIATION IN D_{CNT}

Circuit Type	Operation		Average Power Consumption	Delay	PDP
TSRAM 1	Write	Mean (μ)	5.40E-07nW	1.99E-09ps	1.11E-15aJ
		Standard deviation (σ)	9.22E-08nW	3.06E-09ps	1.721E-15aJ
		Variability(σ/μ)	1.71E-01	1.54	1.55
	Read	Mean (μ)	5.11E-07nW	1.17E-09ps	5.98E-16aJ
		Standard deviation (σ)	1.11E-08nW	6.8E-12ps	1.34E-17aJ
		Variability(σ/μ)	2.17E-02	5.81E-03	2.23E-02
TSRAM 2	Write	Mean (μ)	4.03E-07nW	2.57E-09ps	1.04E-15aJ
		Standard deviation (σ)	1.36E-08nW	3.63E-09ps	1.47E-15aJ
		Variability(σ/μ)	3.37E-02	1.41	1.42
	Read	Mean (μ)	3.25E-07nW	6.96E-10ps	1.96E-16aJ
		Standard deviation (σ)	1.19E-08nW	1.81E-10ps	9.07E-17aJ
		Variability(σ/μ)	3.25E-07	2.60E-01	4.62E-01
Proposed Ternary SRAM 1	Write	Mean (μ)	5.45E-07nW	2.09E-09ps	9.68E-16aJ
		Standard deviation (σ)	1.48E-08nW	3.77E-09ps	1.80E-15aJ
		Variability(σ/μ)	2.72E-02	1.8	1.86
	Read	Mean (μ)	5.11E-07nW	1.17E-09ps	5.99E-16aJ
		Standard deviation (σ)	1.13E-08nW	6.77E-12ps	1.39E-17aJ
		Variability(σ/μ)	2.20E-02	5.78E-03	2.33E-02
Proposed Ternary SRAM 2	Write	Mean (μ)	5.92E-07nW	1.43E-09ps	8.53E-16aJ
		Standard deviation (σ)	1.43E-08nW	3E-09ps	1.79E-15aJ
		Variability(σ/μ)	2.41E-02	2.10	2.10
	Read	Mean (μ)	5.10E-07nW	5.61E-10ps	1.93E-16aJ
		Standard deviation (σ)	1.31E-08nW	1.79E-10ps	5.68E-17aJ
		Variability(σ/μ)	2.58E-02	3.19E-01	2.94E-01

TABLE XII
PROCESS VARIATION IN L_{ch}

Circuit Type	Operation		Average Power Consumption	Delay	PDP
TSRAM 1	Write	Mean (μ)	5.82E-07nW	1.58E-10ps	9.18E-17aJ
		Standard deviation (σ)	1.90E-09nW	3.47E-12ps	2.07E-18aJ
		Variability(σ/μ)	3.07E+02	4.53E+01	4.44E+01
	Read	Mean (μ)	5.55E-07nW	1.16E-09ps	6.47E-16aJ
		Standard deviation (σ)	1.01E-09nW	4.27E-12ps	2.59E-18aJ
		Variability(σ/μ)	1.83E-03	3.67E-03	4.01E-03
TSRAM 2	Write	Mean (μ)	4.31E-07nW	1.02E-10ps	4.37E-17aJ
		Standard deviation (σ)	2.26E-09nW	2.70E-11ps	1.17E-17aJ
		Variability(σ/μ)	1.90E+02	3.76E+00	3.74E+00
	Read	Mean (μ)	4.47E-07nW	8.76E-10ps	6.47E-16aJ
		Standard deviation (σ)	6.28E-10nW	6.19E-13ps	2.59E-18aJ
		Variability(σ/μ)	1.40E-03	7.07E-04	4.01E-03
Proposed Ternary SRAM 1	Write	Mean (μ)	5.89E-07nW	1.58E-10ps	9.32E-17aJ
		Standard deviation (σ)	1.85E-09nW	4E-12ps	2.38E-18aJ
		Variability(σ/μ)	3.19E+02	3.96E+01	3.92E+01
	Read	Mean (μ)	5.55E-07nW	1.16E-09ps	6.47E-16aJ
		Standard deviation (σ)	1.01E-09aJ	4.47E-12ps	2.79E-18aJ
		Variability(σ/μ)	1.82E-03	3.84E-03	4.32E-03
Proposed Ternary SRAM 2	Write	Mean (μ)	6.41E-07nW	9.81E-11ps	6.28E-17aJ
		Standard deviation (σ)	2.33E-09nW	4.38E-12ps	2.66E-18aJ
		Variability(σ/μ)	2.75E+02	2.23E+01	2.36E+01
	Read	Mean (μ)	8.59E-07nW	6.90E-10ps	2.35E-16aJ
		Standard deviation (σ)	1.59E-09nW	2.45E-11aJ	4.6E-19aJ
		Variability(σ/μ)	1.85E-03	3.55E-02	1.96E-03

be observed that, with variation in D_{CNT}, during the write operation, the minimum standard deviation of average power consumption is observed in TSRAM 2, the minimum standard deviation in the delay is observed in the proposed ternary SRAM 2. The minimum standard deviation in PDP is observed in TSRAM 2.

The minimum standard deviation in power consumption during the read operation is observed in the TSRAM 1, and

TABLE XIII
READ OPERATION OF PROPOSED SRAM 2

Design Type	D_{CNT} variation		L_{ch} variation	
	Maximum SNM(mV)	Minimum SNM(mV)	Maximum SNM(mV)	Minimum SNM(mV)
TSRAM 1	141.11	81.98	161.24	112.81
TSRAM 2	138.07	83.38	164.95	112.7
Proposed Ternary SRAM1	98.81	55.48	169.73	112.23
Proposed Ternary SRAM 2	133.78	96.9	161.44	112.51

the minimum standard deviation in the delay is observed in the TSRAM 1 and proposed ternary SRAM 1. The D_{CNT} variations affected TSRAM 1 and proposed SRAM 1 equally during the read operation.

From Table XII, it can be observed that, with variation in L_{ch}, the minimum standard deviation of average power consumption is observed in the proposed SRAM 1. The standard deviation in delay and PDP of proposed design 1 and proposed design 2 are similar and minimum among the discussed designs.

Due to variation in L_{ch}, the minimum standard deviation of power consumption and delay during the read operation is observed in the TSRAM 2, and the minimum standard deviation in PDP is observed in the proposed ternary SRAM 2.

D. Static Noise Margin (SNM)

The SNM represents the stability of a memory cell, and the SNM is defined by the maximum value of DC noise voltage that can be tolerated by a memory cell without changing the stored bit [18], [21]. The SNM can be graphically found by measuring the smallest diagonal on the butterfly curve plot by drawing the voltage transfer characteristics (VTC). The butterfly is plotted in Fig. 12. The butterfly curve shown in Fig. 12, plotted by varying the D_{CNT} and L_{ch}. The maximum and minimum values of the SNM with variation in D_{CNT} and L_{ch} are given in Table XIII. Observation of Table XIII shows that with D_{CNT} , the TSRAM1 shows the maximum value of SNM; the minimum value of SNM is shown by proposed ternary SRAM 1. The variation in both the proposed SRAMs noted minimum and the proposed design 2 shows the minimum difference of 36.88mV; this concludes that the SNM of the proposed design is less affected among all the designs. With L_{ch} variation, the maximum value of SNM observed in the proposed SRAM 1, the proposed SRAM 2, and TSRAM 1 maximum SNM values are equal and minimum among all the designs. The minimum values of SNM are almost equal in all the designs.

V. CONCLUSION

In this article, we have proposed two ternary SRAM designs based on the existing SRAM designs. The designs deal with the typical problem of traditional ternary SRAM's inverters, in which the delay while writing and reading the trit takes a longer time than the binary memory cells. The proposed designs have used the modified ternary inverter to speed up storing and reading the trit to and from the cells, respectively. Due to this, the proposed SRAM cells have acted faster to read and write operations with the expense of power consumption; however, the PDP is less in the proposed designs. Since it has been challenging to obtain exact values of the diameter of carbon nanotube (D_{CNT}) and length of CNFET (L_{ch}), and these process variations affect the circuit designs' performance. Therefore the Monte-Carlo analysis has been conducted on the existing and the proposed designs to know the effect of these process variations on the designs' performance. The read delay of proposed SRAM cell 1 is least and equally affected as the existing design; the write delay with PDP of proposed SRAM cell 2 has been least affected due to variation in D_{CNT}. Due to the variation in the L_{ch}, the write delay of the proposed SRAM cell 2 affected least with PDP of both the proposed designs, during the read operation the variations in PDP of proposed design 2 found minimum. The static noise margin (SNM), which is a measure of the stability of the SRAM cell, has calculated by the graphical method and effects of variations in D_{CNT} observed on SNM. The minimum variation has shown by proposed SRAM cell 2. Therefore, the proposed SRAM cells have provided a solution to the extensive delay problem of ternary memory cells with stability.

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REFERENCES

[1] P. C. Balla and A. Antoniou, "Low power dissipation MOS ternary logic family," *IEEE J. Solid-State Circuits*, vol. 19, no. 5, pp. 739–749, Oct. 1984.
[2] H. N. Shivashankar and A. P. Shivaprasad, "Ternary adder and subtracter using ternary multiplexer," *Int. J. Electron.*, vol. 54, no. 2, pp. 201–209, 1983.
[3] A. P. Dhande and V. T. Ingole, "Design and implementation of 2-bit ternary ALU slice," *Proc. IEEE Int. Conf. Sci. Electron. Technol. Inf. Telecommun.*, 2005, pp. 17–21.
[4] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, "Logic circuits with carbon nanotube transistors," *Science*, vol. 294, no. 5545, pp. 1317–1320, Nov. 2001.
[5] J. T. Butler, "Multiple-valued logic examining its use in ultra-high speed computation," *IEEE Potentials*, vol. 14, no. 2, pp. 11–14, Apr./May 1995.
[6] A. Heung and H. T. Mouftah, "Depletion/enhancement CMOS for a lower power family of three-valued logic circuits," *IEEE J. Solid-State Circuits*, vol. 20, no. 2, pp. 609–616, Apr. 1985.
[7] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Trans. Electron. Devices*, vol. 50, no. 9, pp. 1853–1864, Sep. 2003.
[8] J. Appenzeller, "Carbon nanotubes for high-performance electronics—Progress and prospect," *Proc. IEEE*, vol. 96, no. 2, pp. 201–211, Feb. 2008.

[9] A. Akturk, G. Pennington, N. Goldsman, and A. Wickeden, "Electron transport and velocity oscillations in a carbon nanotube," *IEEE Trans. Nanotechnol.*, vol. 6, no. 4, pp. 469–474, Jul. 2007.
[10] (2008). *Stanford University CNTFET Model Website*. [Online]. Available: http://nano.stanford.edu/model.php?id=23
[11] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nanoidealities and its application—Part I: Model of the intrinsic channel region," *IEEE Trans. Electron Device*, vol. 54, no. 12, pp. 3186–3194, Dec. 2007.
[12] Y.-M. Lin, J. Appenzeller, J. Konch, and P. Avouris, "High-performance carbon nanotube field-effect transistor with tunable polarities," *IEEE Trans. Nanotechnol.*, vol. 4, no. 5, pp. 481–489, Sep. 2005.
[13] Y. Ohno, S. Kishimoto, T. Mizutani, T. Okazaki, and H. Shinohara, "Chirality assignment of individual single-walled carbon nanotubes in carbon nanotube field effect transistors by micro-photocurrent spectroscopy," *Appl. Phys. Lett.*, vol. 84, no. 8, pp. 1368–1370, Feb. 2004.
[14] A. Lin *et al.*, "Threshold voltage and on-off ratio tuning for multiple-tube carbon nanotube FETs," *IEEE Trans. Nanotechnol.*, vol. 8, no. 1, pp. 4–9, Jan. 2009.
[15] A. Raychowdhury and K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design," *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, pp. 168–179, Mar. 2005.
[16] S. C. Kleene, *Introduction to Mathematics*. Amsterdam, The Netherlands: North Holland, 1952, pp. 332–340.
[17] S. Lin, Y.-B. Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 217–225, Mar. 2011.
[18] S. Lin, Y.-B. Kim, and F. Lombardi, "Design of a ternary memory cell using CNTFETs," *IEEE Trans. Nanotechnol.*, vol. 11, no. 5, pp. 1019–1025, Sep. 2012.
[19] K. El Shabrawy, K. Maharatna, D. Bagnall, and B. M. Al-Hashimi, "Modeling SWCNT bandgap and effective mass variation using a Monte Carlo approach," *IEEE Trans. Nanotechnol.*, vol. 9, no. 2, pp. 184–193, Mar. 2010.
[20] C. Vudadha, S. Rajagopalan, A. Dusi, P. S. Phaneendra, and M. B. Srinivas, "Encoder-based optimization of CNFET-based ternary logic circuits," *IEEE Trans. Nanotechnol.*, vol. 17, no. 2, pp. 299–310, Mar. 2018.
[21] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, Oct. 1987.
[22] G. Cho and F. Lombardi, "Design and process variation analysis of CNFET-based ternary memory cell," *Integration* vol. 54, pp. 97–108, Jun. 2016.
[23] M. H. Moaiyeri, A. Doostaregan, and K. Navi, "Design of energy-efficient and robust ternary circuits for nanotechnology," *IET Circuits Devices Syst.*, vol. 5, no. 4, pp. 285–296, 2011.
[24] P. K. Patel, M. M. Malik, and T. K. Gupta, "Performance evaluation of single ended disturb free CNTFET based multi-Vt SRAM," *Microelectron. J.* vol. 90, pp. 19–28, Aug. 2019.
[25] P. K. Patel, M. M. Malik, and T. K. Gupta, "Reliable high-yield CNTFET-based 9T SRAM operating near threshold voltage region," *J. Comput. Electron.*, vol. 17, pp. 774–783, Feb. 2018.

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