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1–20 GHz distributed power amplifier based on shared artificial transmission lines

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Abstract: A 1–20 GHz distributed power amplifier (DPA) with a novel compact structure is designed and implemented in a commercial 0.18 µm CMOS technology. The proposed DPA consists of two distributed amplifiers (DAs), which have separate input artificial transmission lines (ATLs) but with their output ATLs shared to achieve high output power and efficiency in the wide frequency band. The gradually changed output ATL is used to further improve the power performance. Measurement results show that the DPA achieves 9.6 dB average associated gain from 1 to 20 GHz. The output power at 1-dB output compression point (OP_{1dB}) is more than 8.2 dBm, and the peak power-added efficiency (PAE) is 9.6% with the OP_{1dB} of 12.9 dBm at 4 GHz.

Keywords: distributed amplifier, artificial transmission line, power-added efficiency

Classification: Integrated circuits

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1 Introduction

The rapid development of wireless and optical communications makes the total bandwidth of the commercial mobile communication technology cover a wide bandwidth more than one octave, and the low cost is expected for the base-station transceivers, which drives the high efficiency and broadband power amplifier (PA) [1]. Distributed amplifiers (DAs) provide an effective approach for extending the bandwidth and therefore are widely used in the design of ultra-wideband systems. With the process down-scaling and the cutoff frequency extending beyond 100 GHz, CMOS technology has the advantages of integration with other radio frequency (RF) and baseband circuits on the same substrate toward system on chip (SoC) as compared to GaAs PHEMT technology [2, 3] and GaN HEMT technology [4, 5, 6, 7], and it becomes promising to design wideband DA on CMOS. One major deficiency of most reported CMOS DAs [7, 8, 9] is their low output power and efficiency due to the low breakdown voltage and the high silicon substrate loss, which impedes them to be integrated as PAs in SOC.

In this Letter, we present a novel wideband CMOS distributed power amplifier (DPA) based on shared artificial transmission lines (ATLs). The DPA consists of two ATL based DAs in a compact structure, and the gradually changed output ATL further improves the power performance. The fabricated DPA achieves more than 8.2 dBm output power at 1-dB output compression point (OP_{1dB}) with the power-added efficiency (PAE) of 3.5–9.6% in the frequency band of 1–20 GHz.

2 Circuit design and simulation

As shown in Fig. 1, the schematic of the proposed DPA consists of two DAs, which have separate input artificial transmission lines (ATLs) but with a shared ATL in their outputs.

According to the transmission line theory, the characteristic impedance Z_0 of the input or output ATL in DAs is given as

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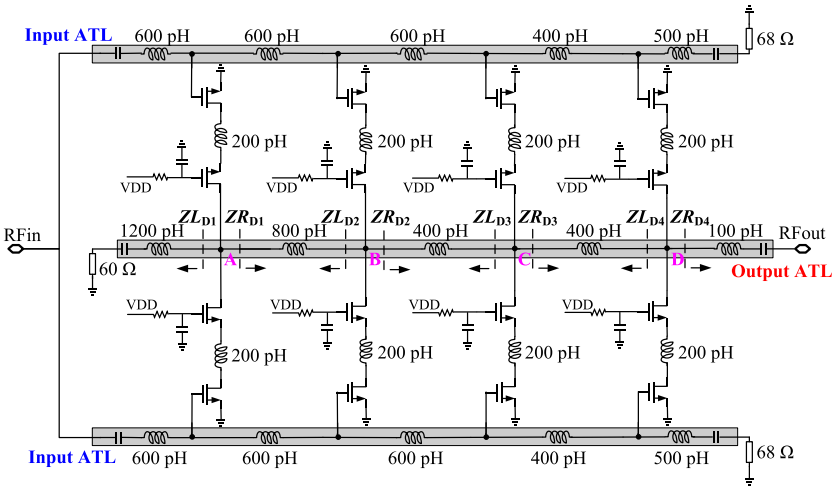

Fig. 1. Schematic diagram of proposed DPA

$$Z_0 = \sqrt{\frac{L_g}{C_{in}}} = \sqrt{\frac{L_d}{C_{out}}} \tag{1}$$

where C_{in} and C_{out} are the input and output parasitic capacitance of gain cells, respectively; L_g and L_d are the on-chip inductor of input and output ATLs, respectively. The bandwidth of DAs is mainly restricted by the cutoff frequency f_c of input and output ATLs:

$$f_c = \frac{1}{2\pi\sqrt{L_g C_{in}}} = \frac{1}{2\pi\sqrt{L_d C_{out}}} \tag{2}$$

According to Eq. (1) and Eq. (2), the cutoff frequency f_c decreases with the increase of C_{in} (C_{out}). However, the transistors in DPAs need to be large enough to provide high transconductance and output power, which results in the large parasitic capacitance, and thus a narrow bandwidth. Furthermore, C_{in} is usually larger than C_{out} and acts as the most important limiting factor for bandwidth. For example, the gate width of transistors in the cascode gain cell is set as 120 µm, and the input and output parasitic capacitance of the gain cell are presented in Fig. 2. It is apparent that the input parasitic capacitance is more than twice as large as the output one.

There are two separate input ATLs and one output ATL in the proposed DPA, as shown in Fig. 1. The equivalent capacitance at the nodes of A~D in the output ATL is twice as large as the output parasitic capacitance of each gain cell, and therefore it releases the bandwidth constraint due to the imbalance of the input and output parasitic capacitance of gain cells. The output current at each node of A~D is also twice as large as the output current of each gain cell, so the gate width of all transistors in Fig. 1 shrinks to 60 µm to reduce the parasitic capacitance in the ATLs, while maintaining the same transconductance and output power of single gain cell in which the transistors are with 120 µm gate width. Since two input ATLs are separate and connected in parallel at the input port, non-uniform input ATLs are designed to make their input impedances close to 100 Ω instead of 50 Ω. The output power of the DPA is the accumulation of the output power of each gain cell. In Fig. 1, ZL_{Di} and ZR_{Di} (the subscript i is from 1 to 4) are the impedance seen

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leftwards and rightwards at the output point of each gain cell, which are connected in parallel between the output point of each gain cell and the ground. According to Norton's theorem, more power will flow rightwards and reach the output port if ZL_{Di} is larger than ZR_{Di} for the same parallel impedance consisting of ZL_{Di} and ZR_{Di}. Hence the on-chip inductors L_{Di} reduces from 1200 pH to 100 pH gradually from the left to the right output port, as shown in Fig. 1. Fig. 3 shows the corresponding impedances ZL_{Di} and ZR_{Di}. It can be seen that ZL_{Di} (solid lines) is larger than ZR_{Di} (dashed lines) in the desired frequency band except some narrow frequency band, which is due to the requirement of the output impedance matching.

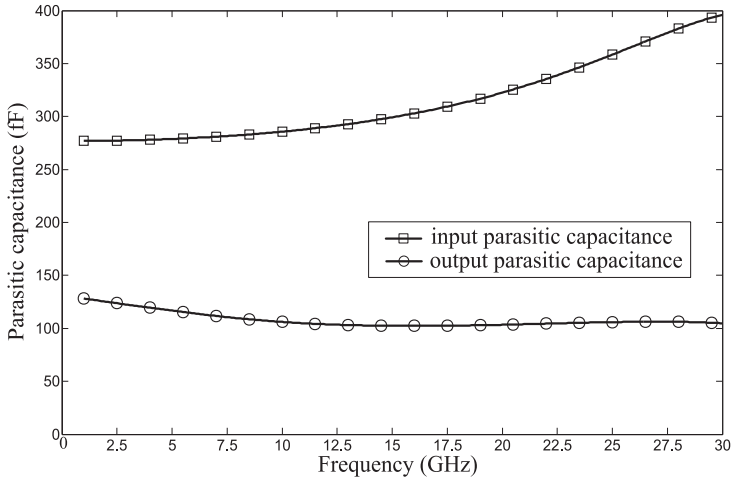

Fig. 2. Input and output parasitic capacitance of gain cell

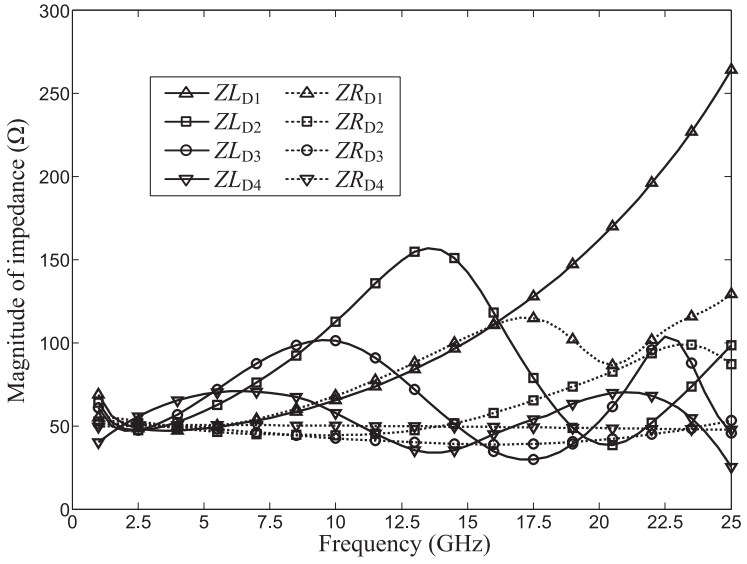

Fig. 3. Impedance at the output point of each gain cell

3 Experimental results and discussion

Fig. 4 is the die photograph of the designed DPA, whose size is 1.32 mm × 0.77 mm containing probe pads. The circuit is measured via on-wafer test.

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The amplifier consumes 168 mW power dissipation with the supply voltage of 2.8 V. Fig. 5 shows the measured S-parameters of the fabricated DPA. The measured average forward gain (S_{21}) is 9.6 dB from 1 to 20 GHz with a peak gain of 10.8 dB at 7.6 GHz. The input return loss (S_{11}) is better than 9.9 dB from 1 to 21 GHz, and the output return loss (S_{22}) is better than 8.3 dB from 1 to 25 GHz. The inaccurate inductor model and unexpected loss in the circuit leads to the acceptable discrepancy between the simulation and the measurement.

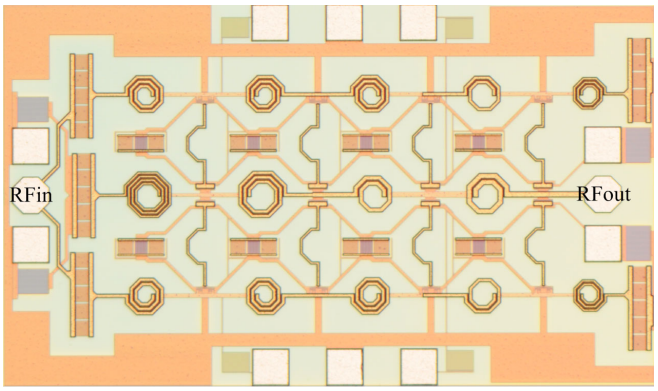

Fig. 4. Die photograph of proposed DPA (chip size: 1.32 mm × 0.77 mm)

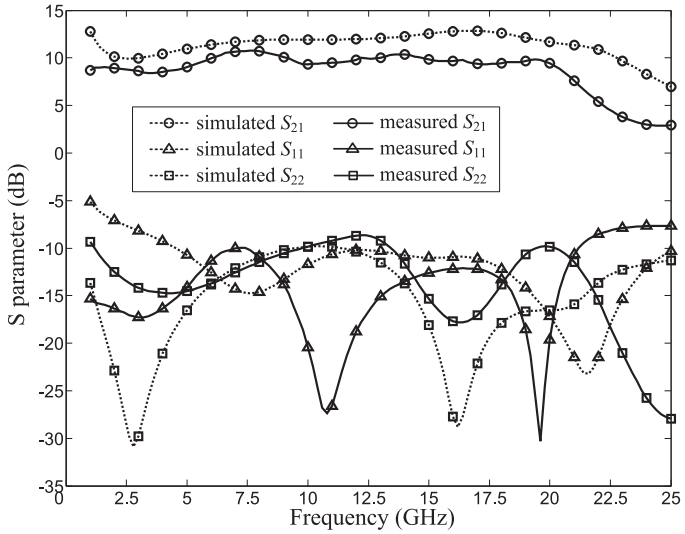

Fig. 5. Measured S-parameter of fabricated DPA at VDD = 2.8 V.

The power measurement shows that the fabricated DPA has a good power performance, which is presented in Fig. 6. The measured OP_{1dB} is from 8.2 to 12.9 dBm in the band of 1–20 GHz while the corresponding PAE is from 3.5% to 9.6%. Finally, Table I summarises the comparison between the fabricated DPA and the previously reported DAs. The proposed DPA exhibits high output OP_{1dB} and good PAE in the wide frequency band.

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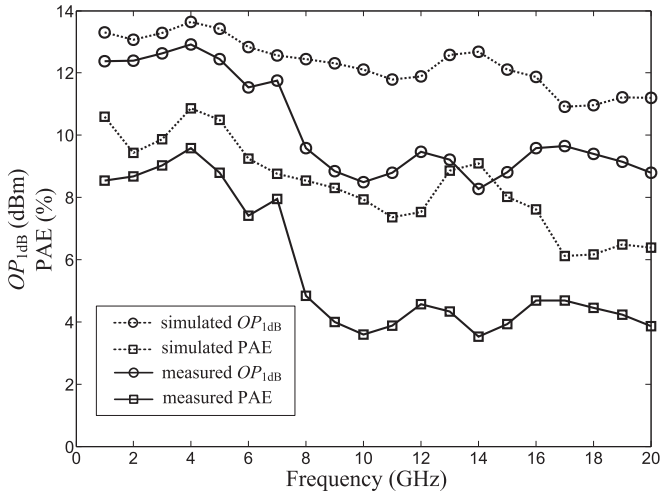

Fig. 6. Measured OP_{1dB} and PAE of fabricated DPA at VDD = 2.8 V

Table I. Performance summary of CMOS DAs

Refs.	[8]	[9]	[10]	This work
Process	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Freq. (GHz)	1.5–34.2	1.5–35.5	22–31	1–20
Gain (dB)	24	25	6.4	9.6
VDD (V)	2.8	2.8	2.6	2.8
PDC (mW)	238	176.4	47	168
OP_{1dB} (dBm)	4.2–9@ 2–30 GHz[a]	4.6–7.4@ 5–35 GHz[a]	4.3–6.5@ 22–30 GHz[a]	8.2–12.9@ 1–20 GHz
PAE (%)[b]	1.1–3@ 2–30 GHz[a]	1.6–3.1@ 5–35 GHz[a]	3.9–6.5@ 22–30 GHz[a]	3.5–9.6@ 1–20 GHz
Area (mm^2)	0.83	0.86	0.17	1.02

a This data is estimated from their papers for comparison.
b PAE is estimated at 1 dB gain compression point.

4 Conclusion

A 1–20 GHz broadband DPA with the OP_{1dB} of more than 8.2 dBm is implemented with a 0.18 µm CMOS technology. The novel compact structure based on shared ATLs and the gradually changed output ATL improve the output power and efficiency while containing the wide operating band. The high output power and good PAE enable the DPA to work as a wideband medium-power PA.

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