Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator

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***Abstract*— The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18-μm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153 μW, respectively. The standard deviation of the input-referred offset is 7.8 mV at 1.2 V supply.**

***Index Terms*— Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), low-power analog design.**

I. Introduction

COMPARATOR is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high-speed ADCs, such as flash ADCs, require high-speed, low-power comparators with small chip area. High-speed comparators in ultra deep submicrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [1]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods [2], [3], techniques employing body-driven transistors [4], [5], current-mode design [6] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock [4], removes the threshold voltage requirement such that body-driven MOSFET operates as a depletion-type device. Based on this approach, in [5], a 1-bit quantizer for sub-1V $\Sigma\Delta$ modulators is proposed. Despite the advantages, the body-driven transistor suffers from smaller transconductance (equal to g_{mb} of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration. Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. In [7]–[9], additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. The proposed comparator of [7] works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes 18 μW. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator first proposed in [10] is based on designing a separate input and cross-coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range [10].

In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in [10], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

The rest of this paper is organized as follows. Section II investigates the operation of the conventional clocked regenerative comparators and the pros and cons of each

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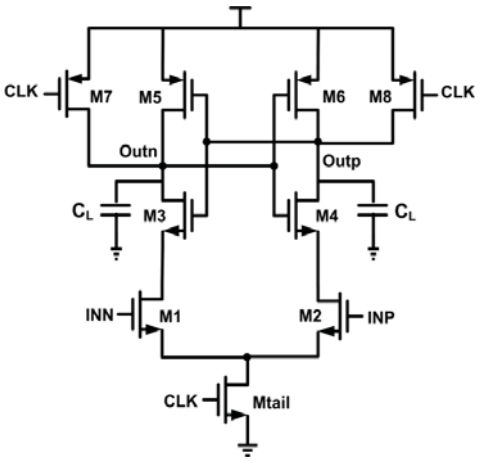

Fig. 1. Schematic diagram of the conventional dynamic comparator.

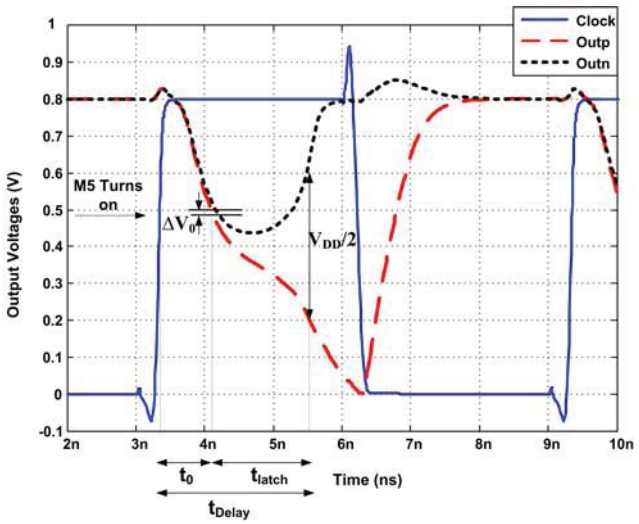

Fig. 2. Transient simulations of the conventional dynamic comparator for input voltage difference of $\Delta V_{\text{in}} = 5$ mV, $V_{\text{cm}} = 0.7$ V, and $V_{\text{DD}} = 0.8$ V.

structure is discussed. Delay analysis is also presented and the analytical expressions for the delay of the comparators are derived. The proposed comparator is presented in Section III. Section IV discusses the design issues. Simulation results are addressed in Section V, followed by conclusions in Section VI.

II. Clocked Regenerative Comparators

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise [11], offset [12], [13], and [14], random decision errors [15], and kick-back noise [16]. In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK $= 0$ and M_{tail} is off, reset transistors (M_7–M_8) pull both output nodes Out$n$ and Out$p$ to V_{DD} to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK $= V_{\text{DD}}$, transistors M_7 and M_8 are off, and M_{tail} is on. Output voltages (Out$p$, Out$n$), which had been pre-charged to V_{DD}, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where $V_{\text{INP}} > V_{\text{INN}}$, Out$p$ discharges faster than Out$n$, hence when Out$p$ (discharged by transistor M_2 drain current), falls down to V_{DD}–$|V_{\text{thp}}|$ before Out$n$ (discharged by transistor M_1 drain current), the corresponding pMOS transistor (M_5) will turn on initiating the latch regeneration caused by back-to-back inverters (M_3, M_5 and M_4, M_6). Thus, Out$n$ pulls to V_{DD} and Out$p$ discharges to ground. If $V_{\text{INP}} < V_{\text{INN}}$, the circuits works vice versa.

As shown in Fig. 2, the delay of this comparator is comprised of two time delays, t_0 and t_{latch}. The delay t_0 represents the capacitive discharge of the load capacitance C_{L} until the first p-channel transistor (M_5/M_6) turns on. In case, the voltage at node INP is bigger than INN (i.e., $V_{\text{INP}} > V_{\text{INN}}$), the drain current of transistor M_2 (I_2) causes faster discharge of Out$p$ node compared to the Out$n$ node, which is driven by M_1 with smaller current. Consequently, the discharge delay (t_0) is given by

$$t_0 = \frac{C_{\text{L}}\,|V_{\text{thp}}|}{I_2} \cong 2\frac{C_{\text{L}}\,|V_{\text{thp}}|}{I_{\text{tail}}}. \tag{1}$$

In (1), since $I_2 = I_{\text{tail}}/2 + \Delta I_{\text{in}} = I_{\text{tail}}/2 + g_{\text{m1,2}}\Delta V_{\text{in}}$, for small differential input (ΔV_{in}), I_2 can be approximated to be constant and equal to the half of the tail current.

The second term, t_{latch}, is the latching delay of two cross-coupled inverters. It is assumed that a voltage swing of $\Delta V_{\text{out}} = V_{\text{DD}}/2$ has to be obtained from an initial output voltage difference ΔV_0 at the falling output (e.g., Out$p$). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch [17]. Hence, the latch delay time is given by, [18]

$$t_{\text{latch}} = \frac{C_{\text{L}}}{g_{m,\text{eff}}} \cdot \ln\left(\frac{\Delta V_{\text{out}}}{\Delta V_0}\right) = \frac{C_{\text{L}}}{g_{m,\text{eff}}} \cdot \ln\left(\frac{V_{\text{DD}}/2}{\Delta V_0}\right) \tag{2}$$

where $g_{m,\text{eff}}$ is the effective transconductance of the back-to-back inverters. In fact, this delay depends, in a logarithmic manner, on the initial output voltage difference at the beginning of the regeneration (i.e., at $t = t_0$). Based on (1), ΔV_0 can be calculated from (3)

$$\begin{aligned}\Delta V_0 &= \left|V_{\text{out}p}(t = t_0) - V_{\text{out}n}(t = t_0)\right| \\ &= \left|V_{\text{thp}}\right| - \frac{I_2 t_0}{C_{\text{L}}} = \left|V_{\text{thp}}\right|\left(1 - \frac{I_2}{I_1}\right).\end{aligned} \tag{3}$$

The current difference, $\Delta I_{\text{in}} = |I_1 - I_2|$, between the branches is much smaller than I_1 and I_2. Thus, I_1 can be

approximated by $I_{\text{tail}}/2$ and (3) can be rewritten as

$$\begin{aligned}\Delta V_0 &= \left|V_{\text{thp}}\right| \frac{\Delta I_{\text{in}}}{I_1} \\ &\approx 2\left|V_{\text{thp}}\right| \frac{\Delta I_{\text{in}}}{I_{\text{tail}}} \\ &= 2\left|V_{\text{thp}}\right| \frac{\sqrt{\beta_{1,2} I_{\text{tail}}}}{I_{\text{tail}}} \Delta V_{\text{in}} \\ &= 2\left|V_{\text{thp}}\right| \sqrt{\frac{\beta_{1,2}}{I_{\text{tail}}}} \Delta V_{\text{in}}. \end{aligned} \tag{4}$$

In this equation, $\beta_{1,2}$ is the input transistors' current factor and I_{tail} is a function of input common-mode voltage (V_{cm}) and V_{DD}. Now, substituting ΔV_0 in latch delay expression and considering t_0, the expression for the delay of the conventional dynamic comparator is obtained as

$$\begin{aligned} t_{\text{delay}} &= t_0 + t_{\text{latch}} \\ &= 2\frac{C_{\text{L}}\left|V_{\text{thp}}\right|}{I_{\text{tail}}} + \frac{C_{\text{L}}}{g_{m,\text{eff}}} \cdot \ln\left(\frac{V_{\text{DD}}}{4\left|V_{\text{thp}}\right| \Delta V_{\text{in}}} \sqrt{\frac{I_{\text{tail}}}{\beta_{1,2}}}\right). \end{aligned} \tag{5}$$

Equation (5) explains the impact of various parameters. The total delay is directly proportional to the comparator load capacitance C_{L} and inversely proportional to the input difference voltage (ΔV_{in}). Besides, the delay depends indirectly to the input common-mode voltage (V_{cm}). By reducing V_{cm}, the delay t_0 of the first sensing phase increases because lower V_{cm} causes smaller bias current (I_{tail}). On the other hand, (4) shows that a delayed discharge with smaller I_{tail} results in an increased initial voltage difference (ΔV_0), reducing t_{latch}. Simulation results show that the effect of reducing the V_{cm} on increasing of t_0 and reducing of t_{latch} will finally lead to an increase in the total delay. In [17], it has been shown that an input common-mode voltage of 70% of the supply voltage is optimal regarding speed and yield.

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch [1]. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M_3 and M_4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M_5 or M_6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M_3 and M_4, where the gate-source voltage of M_5 and M_6 is also small; thus, the delay time of the latch becomes large due to lower transconductances.

Another important drawback of this structure is that there is only one current path, via tail transistor M_{tail}, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch [10]. Besides, as far as M_{tail} operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

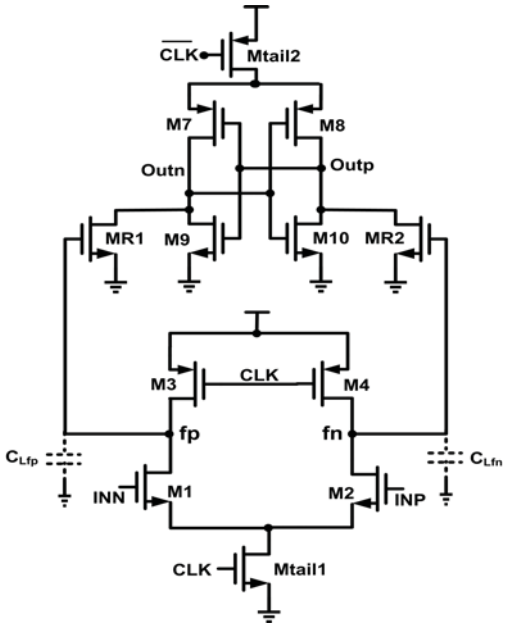

Fig. 3. Schematic diagram of the conventional double-tail dynamic comparator.

B. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator is shown in Fig. 3 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider M_{tail2}, for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the input stage (small M_{tail1}), for low offset [10].

The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK = 0, M_{tail1}, and M_{tail2} are off), transistors M_3-M_4 pre-charge fn and fp nodes to V_{DD}, which in turn causes transistors M_{R1} and M_{R2} to discharge the output nodes to ground. During decision-making phase (CLK = V_{DD}, M_{tail1} and M_{tail2} turn on), M_3-M_4 turn off and voltages at nodes fn and fp start to drop with the rate defined by $I_{\text{Mtail1}}/C_{\text{fn(p)}}$ and on top of this, an input-dependent differential voltage $\Delta V_{\text{fn(p)}}$ will build up. The intermediate stage formed by M_{R1} and M_{R2} passes $\Delta V_{\text{fn(p)}}$ to the cross-coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10].

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t_0 and t_{latch}. The delay t_0 represents the capacitive charging of the load capacitance $C_{L\text{out}}$ (at the latch stage output nodes, Out$n$ and Out$p$) until the first n-channel transistor (M_9/M_{10}) turns on, after which the latch regeneration starts; thus t_0 is obtained

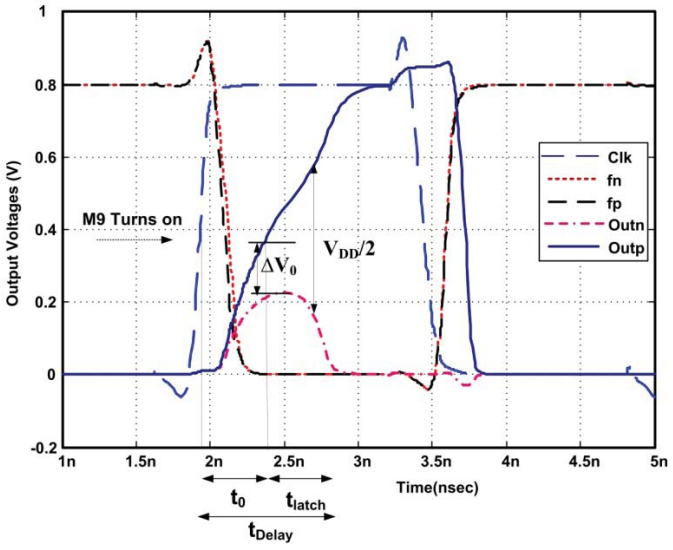

Fig. 4. Transient simulations of the conventional double-tail dynamic comparator for input voltage difference of $\Delta V_{\text{in}} = 5$ mV, $V_{\text{cm}} = 0.7$ V, and $V_{\text{DD}} = 0.8$ V.

from

$$t_0 = \frac{V_{\text{Thn}} C_{L\text{out}}}{I_{\text{B1}}} \approx 2\frac{V_{\text{Thn}} C_{L\text{out}}}{I_{\text{tail2}}} \tag{6}$$

where I_{B1} is the drain current of the M_9 (assuming $V_{\text{INP}} > V_{\text{INN}}$, see Fig. 3) and is approximately equal to the half of the tail current (I_{tail2}).

After the first n-channel transistor of the latch turns on (for instance, M_9), the corresponding output (e.g., Out$n$) will be discharged to the ground, leading front p-channel transistor (e.g., M_8) to turn on, charging another output (Out$p$) to the supply voltage (V_{DD}). The regeneration time (t_{latch}) is achieved according to (2). For the initial output voltage difference at time t_0, ΔV_0 we have

$$\Delta V_0 = \left|V_{\text{out}p}(t = t_0) - V_{\text{out}n}(t = t_0)\right| = V_{\text{Thn}} - \frac{I_{\text{B2}} t_0}{C_{L\text{out}}} = V_{\text{Thn}}\left(1 - \frac{I_{\text{B2}}}{I_{\text{B1}}}\right) \tag{7}$$

where I_{B1} and I_{B2} are the currents of the latch left- and right-side branches of the second stage, respectively.

Considering $\Delta I_{\text{latch}} = |I_{\text{B1}} - I_{\text{B2}}| = g_{mR1,2}\Delta V_{\text{fn/fp}}$, (7) can be rewritten as

$$\Delta V_0 = V_{\text{Thn}}\frac{\Delta I_{\text{latch}}}{I_{\text{B1}}} \approx 2V_{\text{Thn}}\frac{\Delta I_{\text{latch}}}{I_{\text{tail2}}} = 2V_{\text{Thn}}\frac{g_{\text{mR1,2}}}{I_{\text{tail2}}}\Delta V_{\text{fn/fp}} \tag{8}$$

where $g_{\text{mR1,2}}$ is the transconductance of the intermediate stage transistors (M_{R1} and M_{R2}) and $\Delta V_{\text{fn/fp}}$ is the voltage difference at the first stage outputs (fn and fp) at time t_0. Thus, it can be concluded that two main parameters which influence the initial output differential voltage (ΔV_0) and thereby the latch regeneration time are the transconductance of the intermediate stage transistors ($g_{\text{mR1,2}}$) and the voltage difference at the first stage outputs (fn and fp) at time t_0. In fact, intermediate stage transistors amplify the voltage difference of $\Delta V_{\text{fn/fp}}$ causing the latch to be imbalanced.

The differential voltage at nodes fn/fp ($\Delta V_{\text{fn/fp}}$) at time t_0 can be achieved from

$$\begin{aligned}\Delta V_{\text{fn/fp}} &= \left|V_{\text{fn}}(t = t_0) - V_{\text{fp}}(t = t_0)\right| \\ &= t_0 \cdot \frac{I_{\text{N1}} - I_{\text{N2}}}{C_{L,\text{fn(p)}}} \\ &= t_0 \cdot \frac{g_{\text{m1,2}}\Delta V_{\text{in}}}{C_{L,\text{fn(p)}}}.\end{aligned} \tag{9}$$

In this equation, I_{N1} and I_{N2} refer to the discharging currents of input transistors (M_1 and M_2), which are dependent on the input differential voltage (i.e., $\Delta I_{\text{N}} = g_{\text{m1,2}}\Delta V_{\text{in}}$). Substituting (9) in (8), ΔV_0 will be

$$\begin{aligned}\Delta V_0 &= 2V_{\text{Thn}}\frac{g_{\text{mR1,2}}}{I_{\text{tail2}}}\Delta V_{\text{fn/fp}} \\ &= \left(\frac{2V_{\text{Thn}}}{I_{\text{tail2}}}\right)^2 \cdot \frac{C_{L\text{out}}}{C_{L,\text{fn(p)}}} \cdot g_{\text{mR1,2}} g_{\text{m1,2}} \Delta V_{\text{in}}.\end{aligned} \tag{10}$$

This equation shows that ΔV_0 depends strongly on the transconductance of input and intermediate stage transistors, input voltage difference (ΔV_{in}), latch tail current, and the capacitive ratio of $C_{L\text{out}}$ to $C_{L,\text{fn(p)}}$. Substituting ΔV_0 in latch regeneration time (2), the total delay of this comparator is achieved as follows:

$$\begin{aligned}t_{\text{delay}} &= t_0 + t_{\text{latch}} = 2\frac{V_{\text{Thn}} C_{L\text{out}}}{I_{\text{tail2}}} + \frac{C_{L\text{out}}}{g_{m,\text{eff}}} \cdot \ln\left(\frac{V_{\text{DD}}/2}{\Delta V_0}\right) \\ &= 2\frac{V_{\text{Thn}} C_{L\text{out}}}{I_{\text{tail2}}} + \frac{C_{L\text{out}}}{g_{m,\text{eff}}} \\ &\quad \cdot \ln\left(\frac{V_{\text{DD}} \cdot I_{\text{tail2}}^2 \cdot C_{L,\text{fn(p)}}}{8V_{\text{Thn}}^2 \cdot C_{L\text{out}} g_{\text{mR1,2}} g_{\text{m1,2}} \Delta V_{\text{in}}}\right).\end{aligned} \tag{11}$$

From the equations derived for the delay of the double-tail dynamic comparator, some important notes can be concluded.

1) The voltage difference at the first stage outputs ($\Delta V_{\text{fn/fp}}$) at time t_0 has a profound effect on latch initial differential output voltage (ΔV_0) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator.
2) In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to V_{DD}, which means power consumption. The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

III. Proposed Double-Tail Dynamic Comparator

Fig. 5 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase $\Delta V_{\text{fn/fp}}$ in order to increase the latch regeneration speed. For this purpose, two control transistors (M_{c1} and M_{c2}) have been added to the first stage in parallel to M_3/M_4 transistors but in a cross-coupled manner [see Fig. 5(a)].

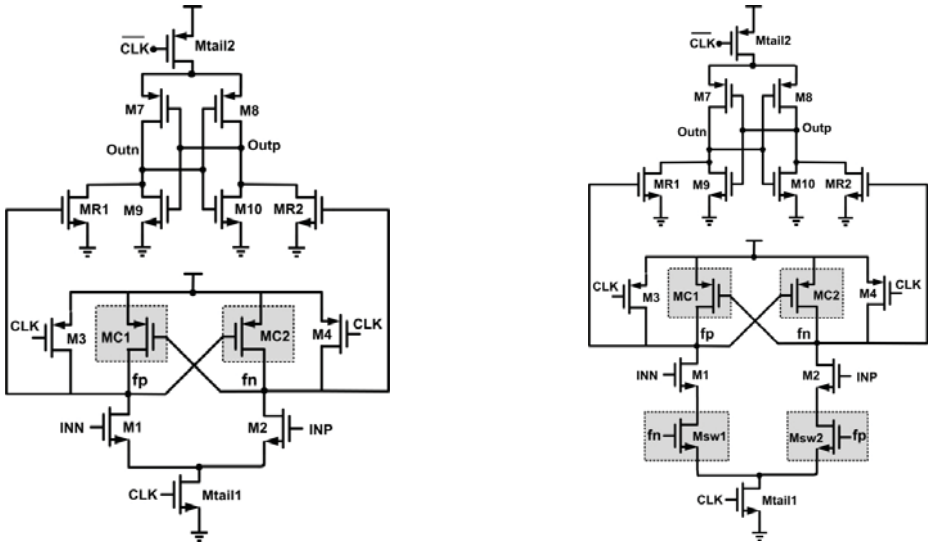

Fig. 5. Schematic diagram of the proposed dynamic comparator. (a) Main idea. (b) Final structure.

A. Operation of the Proposed Comparator

The operation of the proposed comparator is as follows (see Fig. 6). During reset phase (CLK = 0, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both fn and fp nodes to V_{DD}, hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, M_{R1} and M_{R2}, reset both latch outputs to ground.

During decision-making phase (CLK = V_{DD}, M_{tail1}, and M_{tail2} are on), transistors M_3 and M_4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about V_{DD}). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus fn drops faster than fp, (since M_2 provides more current than M_1). As long as fn continues falling, the corresponding pMOS control transistor (M_{c1} in this case) starts to turn on, pulling fp node back to the V_{DD}; so another control transistor (M_{c2}) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which $\Delta V_{fn/fp}$ is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (M_{c1}) turns on, pulling the other node fp back to the V_{DD}. Therefore by the time passing, the difference between fn and fp ($\Delta V_{fn/fp}$) increases in an exponential manner, leading to the reduction of latch regeneration time (this will be shown in Section III-B). Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., M_{c1}) turns on, a current from V_{DD} is drawn to the ground via input and tail transistor (e.g., M_{c1}, $M1$, and M_{tail1}), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [M_{sw1} and M_{sw2}, as shown in Fig. 5(b)].

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to V_{DD} (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the V_{DD} and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from V_{DD}) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch. This will be more discussed in the following section.

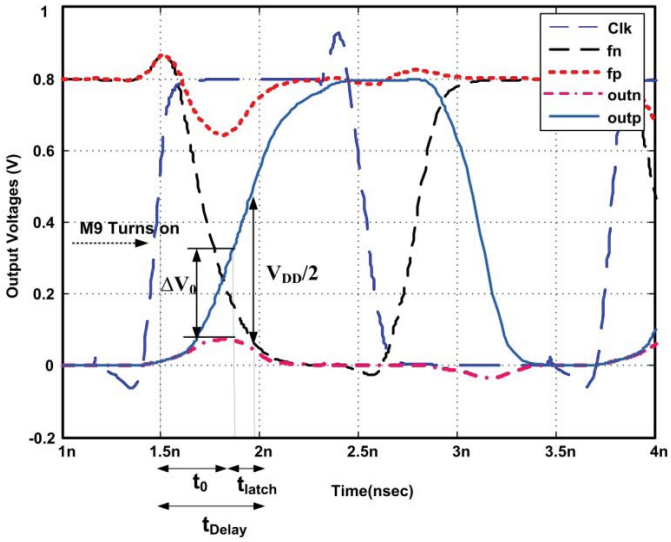

Fig. 6. Transient simulations of the proposed double-tail dynamic comparator for input voltage difference of $\Delta V_{in} = 5$ mV, $V_{cm} = 0.7$ V, and $V_{DD} = 0.8$ V.

B. Delay Analysis

In order to theoretically demonstrate how the delay is reduced, delay equations are derived for this structure as

previously done for the conventional dynamic comparator and the conventional double-tail dynamic comparator. The analysis is similar to the conventional double-tail dynamic comparator, however; the proposed dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference (ΔV_0) at the beginning of the regeneration ($t = t_0$); and second, it enhances the effective transconductace (g_{meff}) of the latch. Each of these factors will be discussed in detail.

1) Effect of Enhancing ΔV_0: As discussed before, we define t_0, as a time after which latch regeneration starts. In other words, t_0 is considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the back-to-back inverters turns on, so that it will pull down one of the outputs and regeneration will commence. According to (2), the latch output voltage difference at time t_0, (ΔV_0) has a considerable impact on the latch regeneration time, such that bigger ΔV_0 results in less regeneration time. Similar to the equation derived for the ΔV_0 of the double-tail structure, in this comparator we have

$$\begin{aligned}\Delta V_0 &= V_{\mathrm{Thn}}\frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{B1}}}\\ &\approx 2V_{\mathrm{Thn}}\frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{tail2}}}\\ &= 2V_{\mathrm{Thn}}\frac{g_{\mathrm{mR1,2}}}{I_{\mathrm{tail2}}}\Delta V_{\mathrm{fn/fp}}.\end{aligned} \tag{12}$$

In order to find $\Delta V_{\mathrm{fn/fp}}$ at $t = t_0$, we shall notice that the combination of the control transistors (M_{c1} and M_{c2}) with two serial switches (M_{sw1}, M_{sw2}) emulates the operation of a back-to-back inverter pair; thus using small-signal model presented in [18], $\Delta V_{\mathrm{fn/fp}}$ is calculated by

$$\Delta V_{\mathrm{fn/fp}} = \Delta V_{\mathrm{fn(p)0}}\exp((A_{\mathrm{v}}-1)t/\tau). \tag{13}$$

In this equation, $\frac{\tau}{A_{\mathrm{v}}-1} \cong \frac{C_{\mathrm{L,fn(p)}}}{G_{\mathrm{m,eff1}}}$ and $\Delta V_{\mathrm{fn(p)0}}$ is the initial fn/fp node difference voltage at the time when the corresponding pMOS control transistor is started to be turned on. Hence, it can be shown that $\Delta V_{\mathrm{fn(p)0}}$ is obtained from

$$\Delta V_{\mathrm{fn(p)0}} = 2\left|V_{\mathrm{Thp}}\right|\frac{g_{\mathrm{m1,2}}\Delta V_{\mathrm{in}}}{I_{\mathrm{tail1}}}. \tag{14}$$

Substituting (13) in (12), ΔV_0 will be

$$\begin{aligned}\Delta V_0 &= 2V_{\mathrm{Thn}}\frac{g_{\mathrm{mR1,2}}}{I_{\mathrm{tail2}}}\Delta V_{\mathrm{fn/fp}}\\ &= 4V_{\mathrm{Thn}}\left|V_{\mathrm{Thp}}\right|\frac{g_{\mathrm{mR1,2}}}{I_{\mathrm{tail2}}}\frac{g_{\mathrm{m1,2}}\Delta V_{\mathrm{in}}}{I_{\mathrm{tail1}}}\exp\left(\frac{G_{\mathrm{m,eff1}}\cdot t_0}{C_{\mathrm{L,fn(p)}}}\right).\end{aligned} \tag{15}$$

Comparing (15) with (10), it is evident that ΔV_0 has been increased remarkably (in an exponential manner) in compare with the conventional dynamic comparator.

2) Effect of Enhancing Latch Effective Transconductance: As mentioned before, in conventional double-tail comparator, both fn and fp nodes will be finally discharged completely. In our proposed comparator, however, the fact that one of the first stage output nodes (fn/fp) will charge up back to the V_{DD} at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective transconductance of the latch is increased. In other words, positive feedback is strengthened. Hence, t_{latch} will be

$$\begin{aligned}t_{\mathrm{latch}} &= \frac{C_{L\mathrm{out}}}{g_{\mathrm{m,eff}}+g_{\mathrm{mR1,2}}}\cdot\ln\left(\frac{\Delta V_{\mathrm{out}}}{\Delta V_0}\right)\\ &= \frac{C_{L\mathrm{out}}}{g_{\mathrm{m,eff}}+g_{\mathrm{mR1,2}}}\cdot\ln\left(\frac{V_{\mathrm{DD}}/2}{\Delta V_0}\right).\end{aligned} \tag{16}$$

Finally, by including both effects, the total delay of the proposed comparator is achieved from

$$\begin{aligned}t_{\mathrm{delay}} &= t_0 + t_{\mathrm{latch}}\\ &= 2\frac{V_{\mathrm{Thn}}C_{L\mathrm{out}}}{I_{\mathrm{tail2}}} + \frac{C_{L\mathrm{out}}}{g_{\mathrm{m,eff}}+g_{\mathrm{mr1,2}}}\cdot\ln\left(\frac{V_{\mathrm{DD}}/2}{\Delta V_0}\right)\\ &= 2\frac{V_{\mathrm{Thn}}C_{L\mathrm{out}}}{I_{\mathrm{tail2}}} + \frac{C_{L\mathrm{out}}}{g_{\mathrm{m,eff}}+g_{\mathrm{mR1,2}}}\\ &\quad\times\ln\left(\frac{V_{\mathrm{DD}}/2}{4V_{\mathrm{Thn}}\left|V_{\mathrm{Thp}}\right|\frac{g_{\mathrm{mR1,2}}}{I_{\mathrm{tail2}}}\frac{g_{\mathrm{m1,2}}\Delta V_{\mathrm{in}}}{I_{\mathrm{tail1}}}\exp\left(\frac{G_{\mathrm{m,eff1}}\cdot t_0}{C_{\mathrm{L,fn(p)}}}\right)}\right).\end{aligned} \tag{17}$$

By comparing the expressions derived for the delay of the three mentioned structures, it can be seen that the proposed comparator takes advantage of an inner positive feedback in double-tail operation, which strengthen the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of $V_{\mathrm{Th}}/V_{\mathrm{DD}}$, the transconductance of the transistors decreases, thus the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator. Simulation results confirm this matter.

3) Reducing the Energy Per Comparison: It is not only the delay parameter which is improved in the modified proposed comparator, but the energy per conversion is reduced as well. As discussed earlier, in conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the V_{DD}. However, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required. This can be seen when being compared with conventional topologies [see Figs. 9(b) and 10(b)].

IV. Design Considerations

In designing the proposed comparator, some design issues must be considered. When determining the size of tail transistors (M_{tail1} and M_{tail2}), it is necessary to ensure that the time it takes that one of the control transistors turns on must be smaller than t_0 (start of regeneration)

$$\begin{aligned}t_{\mathrm{on,Mc1(2)}} < t_0 &\rightarrow \frac{\left|V_{\mathrm{Thp}}\right|\cdot C_{\mathrm{L,fn(p)}}}{I_{\mathrm{n1,2}}} < \frac{V_{\mathrm{Thn}}C_{L\mathrm{out}}}{I_{\mathrm{B1}}}\\ &\rightarrow \frac{\left|V_{\mathrm{Thp}}\right|\cdot C_{\mathrm{L,fn(p)}}}{\frac{I_{\mathrm{Tail1}}}{2}} < \frac{V_{\mathrm{Thn}}\cdot C_{L\mathrm{out}}}{\frac{I_{\mathrm{Tail2}}}{2}}.\end{aligned} \tag{18}$$

This condition can be easily achieved by properly designing the first and second stage tail currents. Even if possible in the fabrication technology, low-threshold pMOS devices can be used as control transistors leading to faster turn on.

In designing the nMOS switches, located below the input transistors, the drain-source voltage of these switches must be considered since it might limit the voltage headroom, restricting the advantage of being used in low-voltage applications. In order to diminish this effect, low-on-resistance nMOS switches are required. In other words, large transistors must be used. Since the parasitic capacitances of these switches do not affect the parasitic capacitances of the fn/fp nodes (delay bottlenecks), it is possible to optimally select the size of the nMOS switch transistors in a way that both low-voltage and low-power operations are maintained.

The effect of mismatch between controlling transistors on the total input-referred offset of the comparator is another important issue. When determining the size of controlling transistors ($M_{C1} - M_{C2}$), two important issues should be considered. First, the effect of threshold voltage mismatch and current factor mismatch of the controlling transistors on the comparator input-referred offset voltage. Second, the effect of transistor sizing on parasitic capacitances of the fn/fp nodes, i.e., $C_{L,fn(p)}$, and consequently the delay of the comparator. While larger transistors are required for better matching; however, the increased parasitic capacitances are delay bottlenecks. In order to study the effect of threshold and current factor mismatch of control transistors on the total input-referred offset voltage, a brief mismatch analysis is presented here.

A. Mismatch Analysis

In principle, the effect of threshold voltage mismatch and current factor mismatch of controlling transistors is almost negligible in most cases except for the situation where input differential voltage (ΔV_{in}) is very small where fn and fp have approximately similar discharging rates. This is true because by the time that the controlling transistor (M_{c1} or M_{C2}) turns on, the differential input signal is already amplified to large amplitude compared to the mismatches. In other words, offset due to the controlling transistor mismatches is divided by the gain from the input to the output. However, in case of small ΔV_{in}, when fn and fp follow each other tightly, the mismatch of the controlling transistors might influence the result of the comparison. Hence, the following brief analyzes the effect of threshold and current factor mismatches of controlling transistors on the total input-referred offset voltage.

1)*Effect of Threshold Voltage Mismatch of* M_{C1}, M_{C2}*, i.e.,* $\Delta V_{ThC1,2}$:

The differential current due to the threshold voltage mismatch can be obtained from

$$i_{diff} = g_{mc1,2}\Delta V_{Thc1,2} \tag{19}$$

where $g_{mc1,2}$ is the transconductance of the controlling transistors. So, the input-referred offset voltage due to the $M_{c1,2}$ threshold voltage mismatch is obtained as follows:

$$\Delta V_{eq,due\,\Delta V_{Thc1,2}} = \frac{g_{mc1,2}\Delta V_{Thc1,2}}{g_{m1,2}} = \frac{\mu_p W_{C1,2} V_{ODC1,2}}{\mu_n W_{1,2} V_{OD1,2}}\Delta V_{Thc1,2} \tag{20}$$

where V_{OD} refers to the overdrive voltage of the transistors.

2)*Effect of Current-Factor Mismatch* M_{C1}, M_{C2}*, i.e.,* $\Delta\beta_{C1,2}$:

In order to calculate the input-referred offset due to the current factor mismatch of $M_{C1,2}$, $\Delta\beta_{C1,2}$ is modeled as a channel width mismatch ΔW, i.e., $\Delta\beta/\beta = \Delta W/W$. The differential current that ΔW generates can be obtained as expressed in (21).

$$i_{diff} = \frac{1}{2}\mu_p C_{ox}\frac{\Delta W}{L}(V_{gsc1,2} - V_{thc1,2})^2. \tag{21}$$

Note that the controlling transistors are in saturation since $|V_{GDc1,2}| = |V_{fn} - V_{fp}| < |V_{thp}|$. So the input-referred offset voltage due to the current factor mismatch is calculated from

$$\Delta V_{eq,due\,\Delta\beta_{C1,2}} = \frac{i_{diff}}{g_{m1,2}} = \frac{0.5\mu_p W_{C1,2}(V_{gsc1,2} - V_{thp})^2}{\mu_n W_{1,2}(V_{gs1,2} - V_{thn})} = \frac{0.5\mu_p W_{C1,2} V_{OD_{C1,2}}^2}{\mu_n W_{1,2}(V_{cm} - R_{CLK}K_{nC1,2}V_{OD_{C1,2}}^2 - V_{thn})} \tag{22}$$

where V_{cm} is the input common mode voltage and R_{clk} is the equivalent on resistance of the tail transistor.

Assuming both mismatch factors, the total input-referred offset due to the mismatch of the controlling transistors can be found from

$$\sigma_{total} = \sqrt{\sigma^2_{\Delta V_{ThC1,2}} + \sigma^2_{\Delta\beta_{C1,2}}}. \tag{23}$$

From (20) and (22), it can be concluded that the ratio of the controlling transistor sizes to the input transistor size, i.e., $(W_{C1,2}/W_{1,2})$, is effective in reducing the offset. Due to the fact that the transconductance of the input transistors ($g_{m1,2}$) is important in amplifying the input differential voltage and due to the dominant role of the size of these transistors on total input-referred offset, usually large input transistors are designed, which results in diminishing the effect of controlling transistors mismatch.

B. Kickback Noise

Principally in latched comparators, the large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called "kickback noise." In [16], it has been shown that the fastest and most power efficient comparators generate more kickback noise. This is true about our proposed dynamic comparator. Although it improves the double-tail

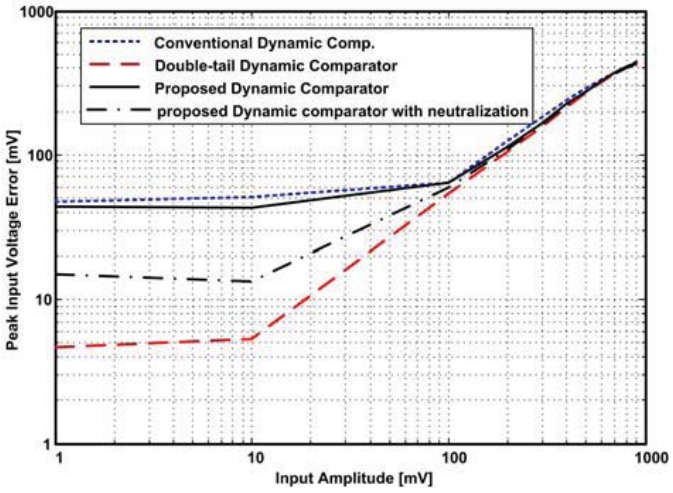

Fig. 7. Peak input voltage error due to kickback noise.

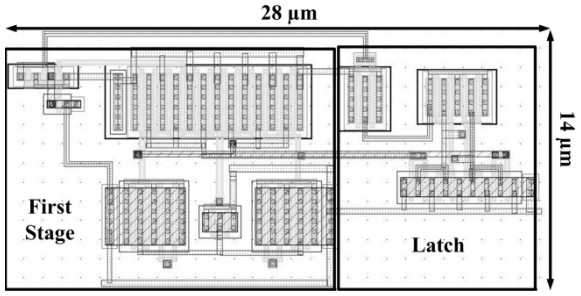

Fig. 8. Layout schematic diagram of the proposed dynamic comparator.

topology in terms of operation speed and thus energy per comparison, the kickback noise is increased in comparison to conventional double-tail structure (Fig. 3). Fig. 7 presents the peak disturbance as a function of differential input voltage of the comparator in three studied architectures. While double-tail structure takes advantage of input-output isolation and thus the minimum kickback noise, the conventional dynamic comparator and our proposed structure has nearly similar kickback noise. However, in our proposed comparator since control transistors are not supposed to be as strong as the latch transistors in conventional dynamic comparator, it is possible to determine the size of those transistors in a way that keeps the advantages of the speed enhancement and power reduction, while reducing kickback noise. Besides, for some applications where kickback becomes important, it is possible to apply simple kickback reduction techniques, such as neutralization [16] to remarkably reduce the kickback noise (See Fig. 7, proposed dynamic comparator with neutralization).

V. Simulation Results

In order to compare the proposed comparator with the conventional and double-tail dynamic comparators, all circuits have been simulated in a 0.18-μm CMOS technology with $V_{\mathrm{DD}} = 1.2$ V. The comparators were optimized and the transistor dimensions were scaled to get an equal offset standard variation of $\sigma_{\mathrm{OS}} = 8$ mV at the input common-mode voltage of $V_{\mathrm{cm}} = 1.1$ V (the same conditions that are found in [10]). Fig. 8 shows the layout of the comparator. Particular care was taken in the layout to avoid affecting delay and power of the comparator. Fig. 9(a) and (b) demonstrates

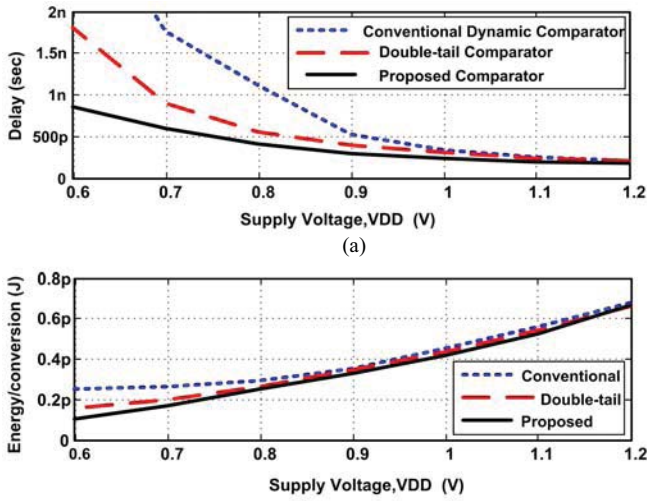

Fig. 9. (a) Post-layout simulated delay and (b) energy per conversion as a function of supply voltage ($\Delta V_{\mathrm{in}} = 50$ mV, $V_{\mathrm{cm}} = V_{\mathrm{DD}} - 0.1$).

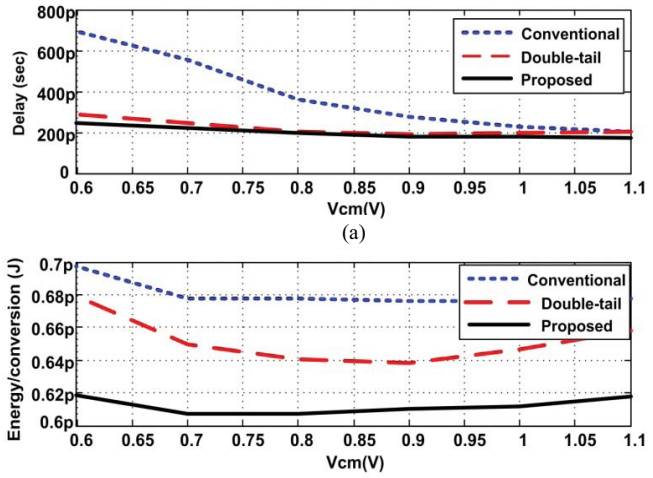

Fig. 10. (a) Post-layout simulated delay and (b) energy per conversion as a function of input common-mode voltage ($\Delta V_{\mathrm{in}} = 50$ mV, $V_{\mathrm{DD}} = 1.2$).

TABLE I
Summary of the Comparator Performance

Item	Value
Technology	180-nm CMOS
Supply voltage	1.2 V
Average power dissipation per conversion @ freq. = 500 MHz	329 μW
Worst case delay ($V_{\mathrm{cm}} = 0.6$ V, $\Delta V_{\mathrm{in}} = 1$ mV)	550 ps
Delay/log(ΔV_{in})	69 ps/dec
Offset standard deviation (1-sigma) (σ_{os})	7.8 mV
Energy efficiency	0.66 pJ

TABLE II
PERFORMANCE COMPARISON

Comparator structure	Conventional Dynamic Comparator	Double-tail Dynamic Comparator	Proposed Dynamic Comparator	
Technology CMOS	180 nm	180 nm	180 nm	
Supply voltage (V)	0.8 V	0.8 V	0.8 V	
Maximum sampling frequency	900 MHz	1.8 GHz	2.4 GHz	
Delay/log(ΔV_{in}) (ps/dec.)	940	358	294	
Peak transient noise voltage at regeneration time(nV)	215 n	221 n	219 n	
Kickback noise voltage (at $\Delta V_{in} = 10$ mV)	51.3 mV	5.3 mV	43 mV	With neutralization: 13 mV
Energy per conversion (J)	0.3 p	0.27 p	0.24 p	Without M_{st01} and M_{st02}: 0.265 p
Input-referred offset voltage (mV)	7.89 mV	7.91 mV	7.8 m	
Estimated area	16 $\mu \times 16$ μ	28 $\mu \times 12$ μ	28 $\mu \times 14$ μ	

the post-layout simulation results of the delay and the energy per conversion of the mentioned dynamic comparators versus supply voltage variation. As shown in Fig. 9(a), in comparison with the other two structures, the delay of the proposed double-tail dynamic comparator is significantly reduced in low-voltage supplies. It is obvious that at high supply voltages, all structures have approximately similar performances, about 200 ps clk-to-output delay (including clock buffer) with 0.65 pJ/bit-conversion for 8-mV offset. However, by decreasing the supply voltage, three structures start to behave differently. It is evident that the double-tail topology can operate faster and can be used in lower supply voltages, while consuming nearly the same power as the conventional dynamic comparator. The case is even much better for the proposed comparator when compared to the conventional double-tail topology. For instance, the proposed comparator can operate in 0.6 V supply at the cost of 106 fJ/conversion with 840 ps delay versus 1.81 ns for the conventional double-tail comparator and 3.5 ns for the conventional topology. Our simulations show that if the circuit is optimized for $V_{DD} = 0.6$ V, the results would be even better for the proposed circuit. Fig. 10 shows the simulated performance as a function of input common-voltage (V_{cm}). Generally in the double-tail topologies, the delay of the comparator is less influenced by the variation of the input common-mode voltage in comparison with the conventional dynamic topology and thus has a wider common-mode range. The power consumption is nearly equal.

Fig. 11 depicts the dependence of the comparator delay on power supply level at various differential input voltages. For $\Delta V_{in} = 10$ mV, the delay is 460 ps at $V_{DD} = 0.9$ V. This delay drops from 460 to 162 ps when V_{DD} changes from 0.9 to 1.5 V. In addition, at a given V_{DD}, the larger the differential input voltage, the smaller the comparator delay will be. Fig. 12 shows the simulated delay of the comparator versus differential input voltage under different conditions of input common-mode voltage (V_{cm}) at $V_{DD} = 1.2$ V. The delay of the comparator at $\Delta V_{in} = 1$ mV and $V_{cm} = 700$ m is 413 ps. For a given value of V_{cm}, the delay decreases as differential input voltage increases. Furthermore, the delay is also dependent on the variation of common-mode voltage. For example, at $\Delta V_{in} = 10$ mV, the delay increases by 64 ps, from 239 to 303 ps, as V_{cm} decreases from 900 to 700 mV. As shown in

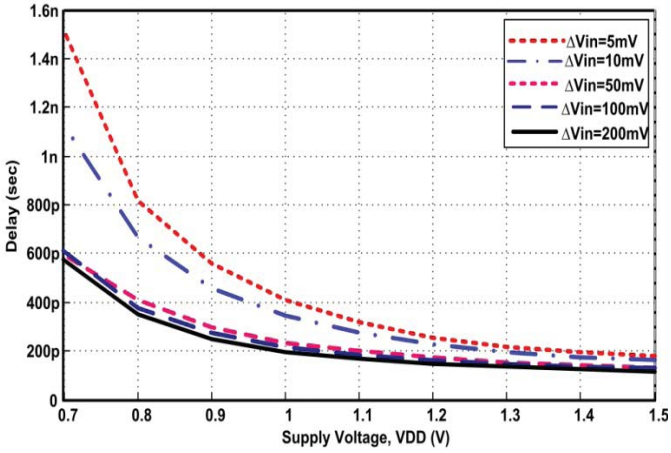

Fig. 11. Delay of the proposed comparator versus supply voltage (V_{DD}).

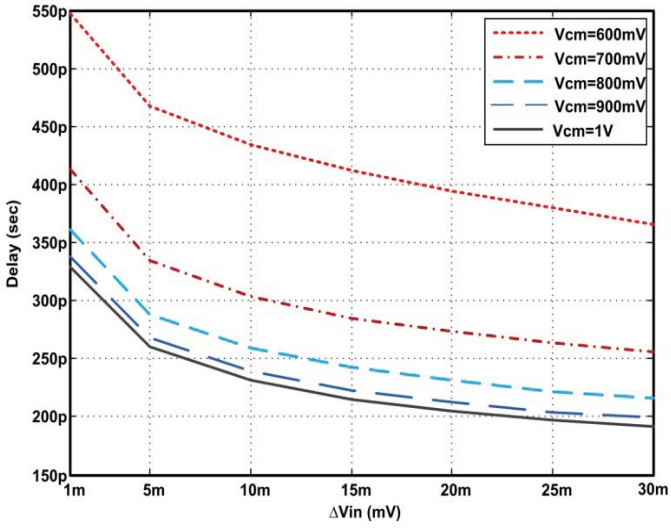

Fig. 12. Delay of the proposed comparator versus input voltage difference (ΔV_{in}).

Fig. 13, the standard deviation of the offset of the proposed comparator is achieved to be $\sigma_{OS} = 7.8$ mV using Monte Carlo simulations for a run of 300 samples. Table I summarizes the performance of the proposed dynamic comparator. Finally,

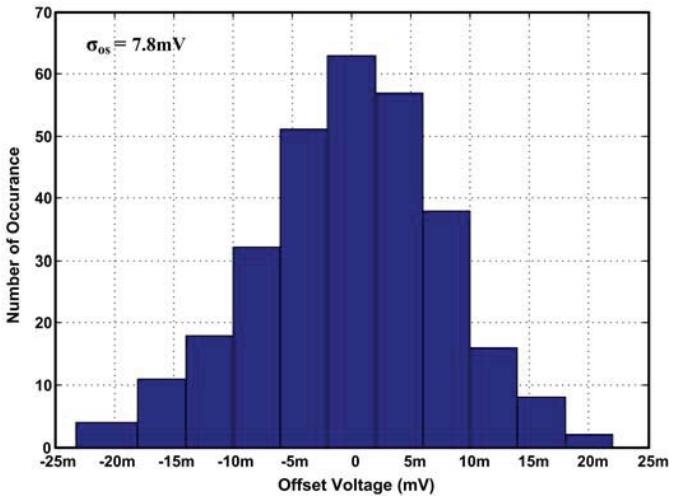

Fig. 13. Histogram diagram of Monte Carlo simulation of the offset in proposed dynamic comparator.

Table II compares the performance of the proposed comparator with the conventional dynamic and double-tail comparators. In 0.18-μm CMOS, the proposed comparator provides the maximum sampling of 2.4 GHz at 0.8-V supply voltage.

VI. Conclusion

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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