A 1-V, 8-Bit Successive Approximation ADC in Standard CMOS Process

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***Abstract*—A 1-V 8-bit 50-kS/s successive approximation analog-to-digital converter (ADC) implemented in a conventional 1.2-μm CMOS process is presented. Low voltage, large signal swing sample-and-hold, and digital-to-analog conversion are realized based on inverting op-amp configurations with biasing currents added to the op-amp negative input terminal so that the op-amp input common-mode voltages can be biased near ground to minimize the supply voltage. At the same time, the input and output quiescent voltages can be set at half of the supply rails. Low-voltage latched comparator is realized based on current-mode approach. The entire ADC including all the digital circuits consumes less than 0.34 mW. An effective number of bits of 7.9 was obtained for a 1-kHz 850-mV peak-to-peak input signal.**

***Index Terms*—Analog-to-digital converter, CMOS, comparator, digital-to-analog converter, low voltage, sample-and-hold.**

I. Introduction

IN MANY mixed-signal systems, analog-to-digital converters (ADC's) are required for interfacing analog signals to digital circuits. The requirement is usually to integrate these ADC's with digital signal processors (DSP's) in a low-cost CMOS technology. However, due to reliability issues, the supply voltages for advanced CMOS processes have been reduced continuously and will reduce down to 1.5 V and below in the near future [1]. As a result, ADC's that are integrated with a DSP are required to operate in the same range of supply voltage. However, designing an ADC to operate at such a low supply voltage presents a great challenge, which comes from the fact that the threshold voltages of MOSFET devices are relatively high for the given supply voltage ranges even for future CMOS processes [1]. To address this challenge, different techniques have been used to realize ADC's including the use of specialized process that provides low-threshold devices [2], bootstrap techniques [3], and switched-op-amp techniques [4]. This paper describes an alternative technique to design a 1-V 8-bit successive approximation ADC in a standard CMOS process. The ADC was designed for low-power, medium-quality applications such as data acquisition. The block diagram of the ADC is shown in Fig. 1. The major analog building blocks are discussed in the following sections.

II. Sample-and-Hold Design

Most CMOS sample-and-holds (S/H's) are based on switched-capacitor techniques. A typical design is shown in Fig. 2. When this S/H is operated at low voltage (e.g., 1 V), the input and output must have large signal swing to maximize the signal-to-noise ratio (SNR). Since the threshold voltages for NMOS and PMOS in a conventional CMOS process are in the range between 0.5–0.9 V, the switches will fail to pass voltage signals in the midrange of the supply rails even if transmission gates are used [5]. Second, for a typical op-amp with a PMOS differential pair as the input stage, the maximum input common-mode voltage of the op-amp is equal to $V_{\rm DD} - |V_{\rm TP}| - 2V_{\rm SDsat}$. For a $|V_{\rm TP}|$ of more than 0.5 V, the input common-mode voltage cannot be set at $V_{\rm DD}/2$ for a 1-V supply. As a result, this S/H is not suitable for low-voltage operation.

A low-voltage S/H that uses resistors is proposed as shown in Fig. 3. When ϕ_1 turns high, the S/H is in sampling mode and is configured as an inverting amplifier with an ac gain of $-R_2/R_1$. Highly linear gain can be achieved using poly resistors. Since the input and output of the S/H are connected to resistors, the signal swing can be close to the supply rails. Furthermore, the holding capacitor C is acting as a capacitive load to the op-amp. Hence, the bandwidth $\omega_{-3\ \rm dB}$ is almost independent of C and is given as $\omega_T/[1 + R_2/(R_1//r_{\rm ds1})]$, where ω_T is the unity-gain frequency of the op-amp and $r_{\rm ds1}$ is the output impedance of the current source. A high bandwidth is desired in this mode to minimize the tracking error. The input common-mode voltage of the op-amp is set at v_x, which is about one $V_{\rm DSsat}$ above ground such that M_1 has sufficient $V_{\rm DS}$ to operate as a current source. Using this current source, the input and output quiescent voltages can be set at $V_{\rm DD}/2$ even though v_x is close to ground. The required current can be determined using the following expression:

$$I_1 = \left(\frac{V_{\rm DD}}{2} - v_x\right)\left(\frac{1}{R_2} + \frac{1}{R_1}\right). \tag{1}$$

Since the switches used in the S/H are only required to pass current signals with small voltage drops, they can be realized using NMOS's. The switches will have sufficient overdrive voltage, which is equal to $V_{\rm DD} - V_{\rm TN} - v_x$. The minimum required $V_{\rm DD}$ of the S/H is equal to the maximum input common-mode of the op-amp plus $V_{\rm DSsat1}$ and is approximately equal to $|V_T| + 3V_{\rm DSsat}$. Without I_1, the minimum required $V_{\rm DD}$ is approximately given by $2|V_T| + 4V_{\rm DSsat}$.

During the falling edge of ϕ_1, the op-amp output is sampled by capacitor C. The mean-squared noise on the sampled signal $v_{\rm no}^2$ can be written as

$$v_{\rm no}^2 = \left(\frac{4KT}{R_1} + \frac{4KT}{R_2} + I_n^2\right)R_2^2\frac{\omega_{-3\ \rm dB}}{4} + v_{\rm na}^2\left(1 + \frac{R_2}{R_1//r_{\rm ds1}}\right)^2\frac{\omega_{-3\ \rm dB}}{4} \tag{2}$$

where $v_{\rm na}$ is the input noise voltage of the op-amp and I_n^2 is the mean-squared current noise of I_1 that can be derived

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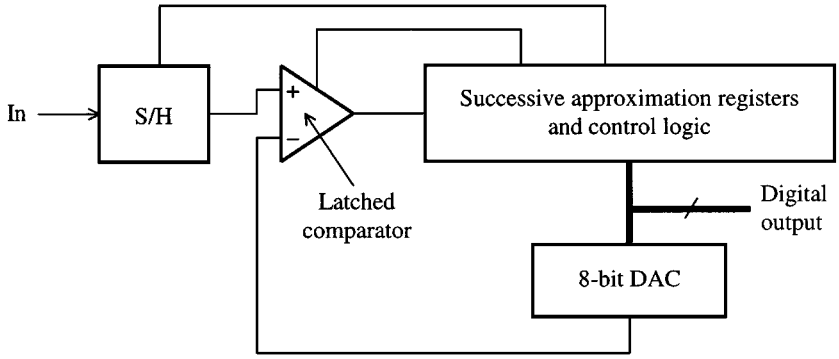

Fig. 1. Block diagram of the successive approximation ADC.

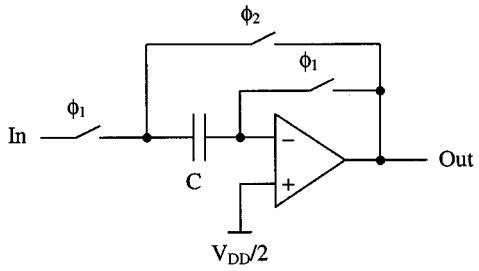

Fig. 2. Typical CMOS S/H.

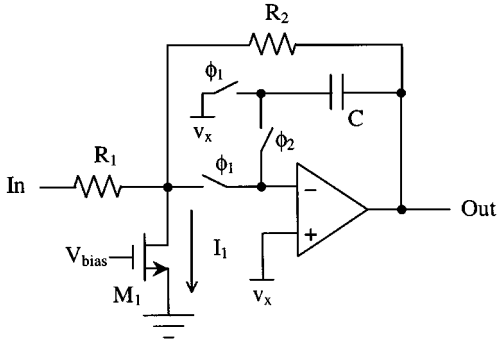

Fig. 3. Proposed low-voltage S/H.

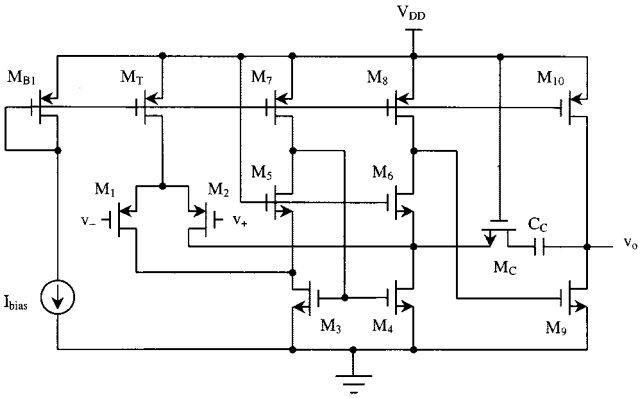

Fig. 4. Two-stage op-amp design.

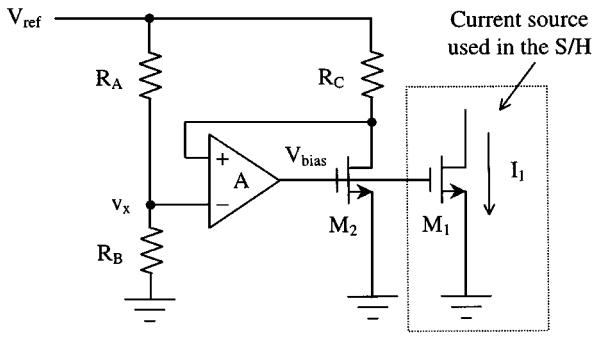

Fig. 5. Biasing circuit for generating the require current used in the S/H.

as 16 KT($V_{\rm DD}/2 - v_x$)/[$3v_x(R_1//R_2)$] when v_x is equal to $V_{\rm DSsat1}$. Although, for a typical design, the term due to $v_{\rm na}$ is usually dominant, the first term will become significant as v_x becomes too small. As a result, there is a slight tradeoff between supply voltage and SNR. When ϕ_2 turns high, the S/H is in hold mode, and the capacitor C is connected between the negative input and the output of the op-amp. Since the op-amp is in unity-gain feedback during this mode, the op-amp output impedance will be reduced by the open-loop gain, and hence, signal feedthrough from the input to the output is attenuated. The overall attenuation is approximately given as $r_o/(R_1+R_2)$, where r_o is the op-amp output impedance divided by the open-loop op-amp gain. The op-amp is designed based on a two-stage design, as shown in Fig. 4. The output stage has been designed to have a large enough biasing current such that the output can swing close to the supply rails for a given resistance load. The minimum supply voltage for the op-amp is given by $\max\{V_{\rm TN5}+V_{\rm DSsat5}+V_{\rm DSsat3},\ V_{\rm SDsat7}+V_{\rm DSsat5}+V_{\rm DSsat3}\}$. Using this op-amp, the signal feedthrough of the S/H is estimated to be less than -52 dB. Although a low-output-impedance op-amp can further reduce the signal feedthrough and increase the driving capability, either the bandwidth during sampling mode or the output swing will be reduced in this case.

Nonlinearity errors of the S/H due to signal-dependent charge injection of the switches are minimized since the drain and source voltages of the switches are always connected to the same potential v_x. However, clock feedthrough and charge injection due to the switches will produce an offset voltage and hence, affect the overall offset error of the ADC. Depending on the applications, this offset error may not be of concern.

To design the S/H that can track with process variation, the current source used for biasing the S/H must track with variations in resistor values using a biasing circuit shown in Fig. 5.

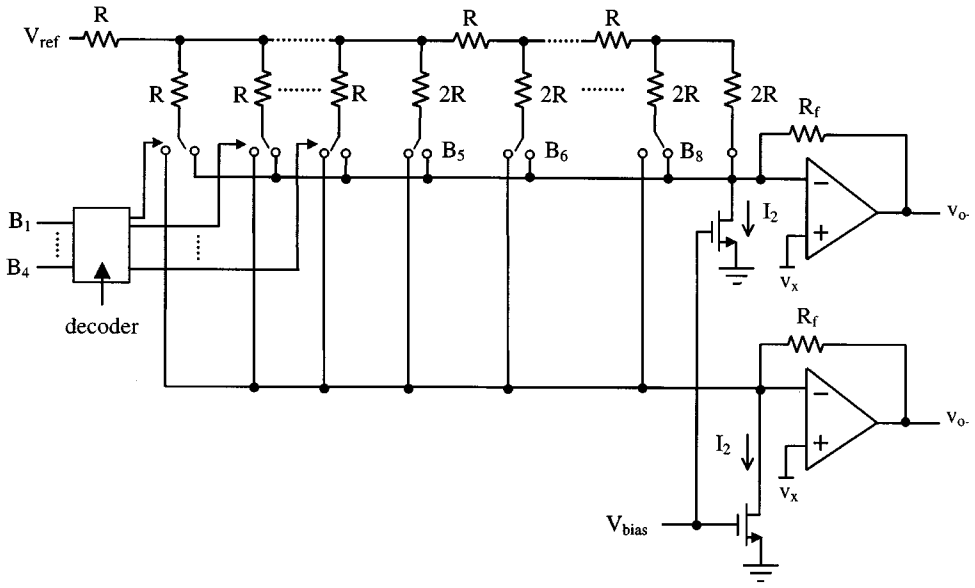

Fig. 6. Low-voltage DAC design.

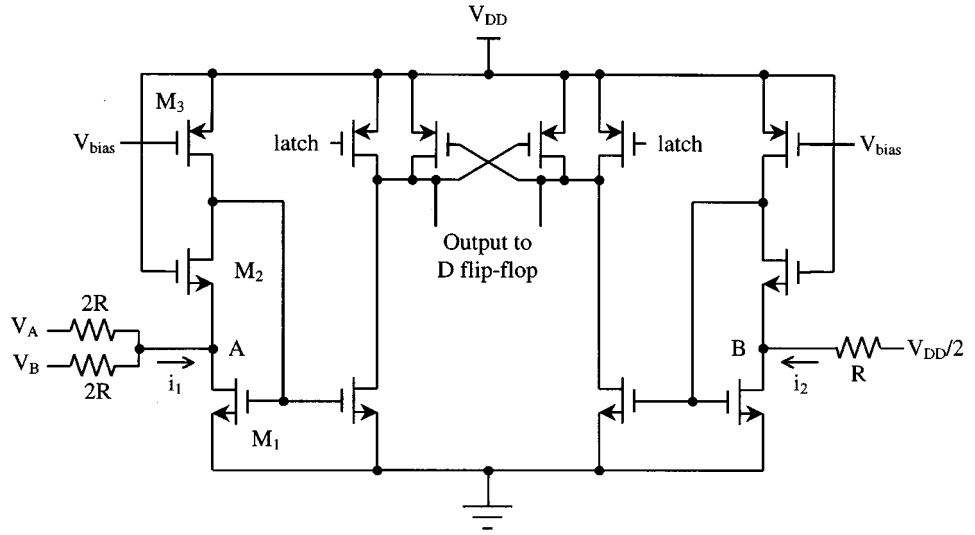

Fig. 7. Low-voltage latched comparator using current-mode approach.

The resistors R_A and R_B are used for generating the op-amp input common-mode voltage v_x from a given fixed reference voltage $V_{\rm ref}$. Due to the feedback loop consisting of amplifier A, M_2, and R_C, the drain voltage of M_2 is equal to v_x, and the current source I_1 that is used for biasing the S/H is equal to $(V_{\rm ref} - v_x)/R_C$, where R_C can be determined using (1). As a result, I_1 will track with variations in resistor values. Notice that the drain voltages of M_1 and M_2 have the same potential equal to v_x, and their drain currents will be the same even if both M_1 and M_2 are in triode region. Therefore, v_x can be set robustly close to ground. The amplifier A can be realized as the first stage of the op-amp shown in Fig. 4. Fully differential implementation of the S/H is also possible by adding an extra current source to the positive terminal of the fully differential op-amp. However, a slightly different biasing circuit to control the current sources for keeping the op-amp input common-mode voltage close to ground is required.

III. Digital-to-Analog Design

In the literature, different digital-to-analog converter (DAC) techniques have been reported. However, they may not be suitable for low-voltage design. The DAC required in the ADC is designed based on an R-2R ladder (Fig. 6). Although only one op-amp is actually required, two op-amps are used so that one of the outputs can be used for measuring the performance of the DAC. To operate the DAC at 1-V supply, the negative input terminals of the op-amps are biased using two current sources I_2's such that the op-amp input common-mode voltages can be set close to ground and the switches can have sufficient overdrive voltages, as discussed in Section II. To relax the matching requirement of the resistors and to minimize the magnitude of glitches, the four most significant-bit resistors are realized in one segment from 15 equal resistors using thermometer coding. The sizes of the switches are scaled to accommodate different current levels to minimize the overall DAC nonlinearity.

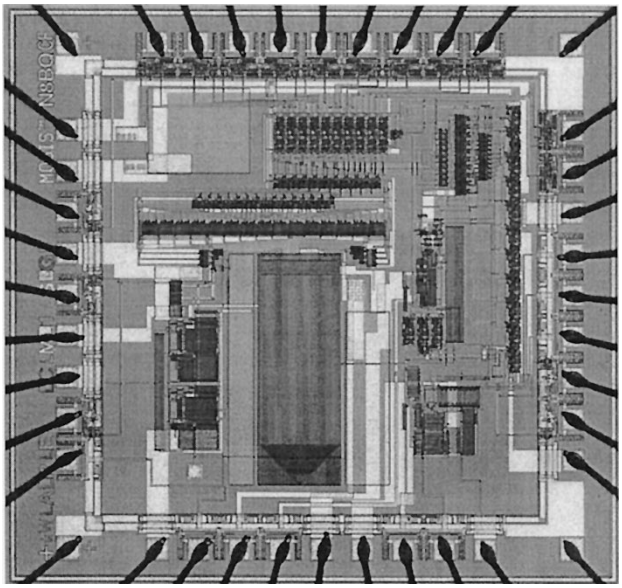

Fig. 8. Die photo.

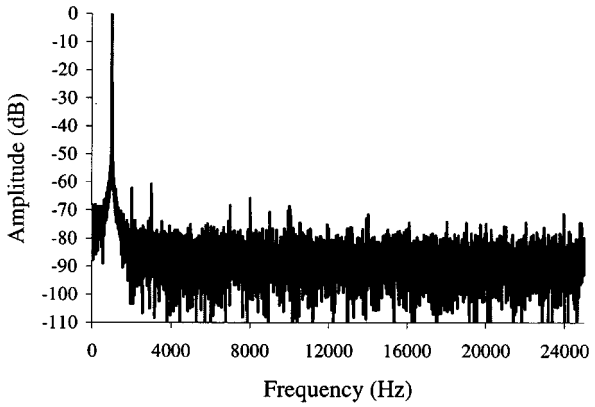

Fig. 9. Measured FFT spectrum for a 1-kHz input sampled at 50 kS/s.

IV. Latched Comparator Design

Conventionally, the comparator is designed to have a differential pair as the input stage. Unfortunately, the input common-mode range is limited for 1-V operation. Furthermore, using switched-capacitor techniques to shift the input voltages to an acceptable input common-mode range before comparison may not be possible since switches cannot be used for passing voltage signals in the midrange of the supply rails. To design a low-voltage latched comparator with wide input swing, a current-mode approach is employed as shown in Fig. 7. Nodes A and B have very low input impedance and can be determined as $1/g_{m1}g_{m2}r_{\rm ds3}$. The quiescent voltage V_Q for both nodes is approximately equal to $V_{\rm DD}-V_{\rm GS2}$. Therefore, the currents i_1 and i_2 flowing to nodes A and B are equal to $[V_A+V_B-2V_Q]/2R$ and $(V_{\rm DD}/2-V_Q)/R$, respectively, where V_A and V_B are connected to the S/H output and the negative DAC output, respectively. Effectively, i_1 is proportional to the voltage difference between the S/H output and the DAC output plus a quiescent current of $(V_{\rm DD}/2-V_Q)/R$, which is due to the voltage difference between the quiescent output voltages of the S/H and the DAC and the voltage at node A. The current i_2 is used for generating a reference current for comparison. When the latch signal turns high, i_1 and i_2 are compared, and a digital signal is generated at the output nodes. Since the comparator inputs are connected to resistors, high input signal swings can be obtained. The minimum supply voltage is given by $\max\{V_{\rm TN2}+V_{\rm DSsat2}+V_{\rm DSsat1},\ V_{\rm SDsat3}+V_{\rm DSsat2}+V_{\rm DSsat1}\}$, which is usually lower than 1 V. The offset of the comparator depends on the mismatch of the MOSFET's and the resistors. However, this offset only affects the overall ADC offset but not the overall linearity.

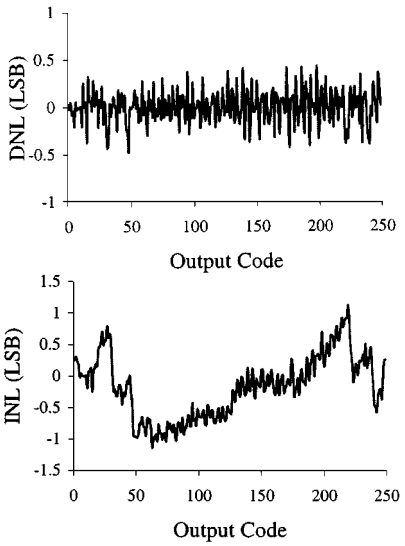

Fig. 10. Measured DNL and INL.

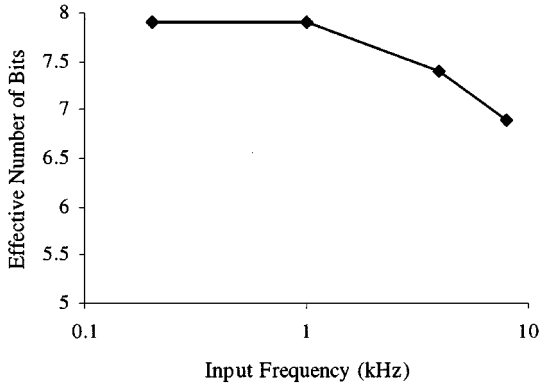

Fig. 11. ENOB versus input frequency.

V. Implementation and Experimental Results

The ADC was fabricated in a conventional 1.2-μm CMOS process with $V_{\rm TN}\approx 0.6$ V and $V_{\rm TP}\approx -0.8$ V. The die photo is shown in Fig. 8. All the poly resistors had values between 20 and 40 kΩ. The holding capacitor in the S/H had a value of about 1.5 pF. To simplify the design of the ADC, the biasing circuit shown in Fig. 5 was omitted in the actual implementation. Instead, external resistors were used for generating the required biasing currents. The DAC was measured to have an output swing between 0.075–0.925 V and an effective number of bits (ENOB) of 7.9 for a 1-kHz input with a sampling rate of 500 kS/s. A separate S/H was fabricated in a different chip. For

TABLE I
MEASURED ADC PERFORMANCE

Supply voltage	1 V
Total power dissipation	0.34 mW
Technology	1.2 μm CMOS ($V_{TN} \approx 0.6$ V, $V_{TP} \approx -0.8$ V)
Sampling rate	50 kS/s
Resolution	8 bits
Active area	$< 1.8 \times 1.8$ mm^2
Input swing	850 mV
DNL	0.47 LSB
INL	1.14 LSB
THD @ f_{in} = 1 kHz	–60.52 dB
SFDR @ f_{in} = 1 kHz	62.87 dB
ENOB @ f_{in} = 1 kHz	7.9 bits

a 50-kHz input with a sampling rate of 500 kS/s, the S/H has a track-mode total harmonic distortion (THD) of about −70 dB and a track-and-hold-mode THD of less than −62 dB for a 0.8-V output swing. The entire ADC, including all the biasing currents, the control logic, and the pad drivers, consumes less than 0.34 mW at 1 V for a sampling rate of 50 kS/s. Each op-amp dissipates about 90 μW. The fast Fourier transform (FFT) spectrum of the digital output signals for a 1-kHz, 850-mV peak-to-peak input signal is shown in Fig. 9. The signal-to-(noise + distortion) ratio was measured to be 47.6 dB, and the corresponding ENOB was 7.9. The differential nonlinearity (DNL) and integral nonlinearity (INL) are plotted in Fig. 10. For low input frequencies, the ENOB is close to the ideal case, as shown in Fig. 11, and drops to 6.9 bits at 8 kHz. This degradation is mainly due to the degradation in the performance of the DAC for high input frequencies. The performance of the ADC is summarized in Table I.

VI. CONCLUSION

Advances in CMOS technology have driven down supply voltages. Integrating mixed-signal systems in these processes requires the digital circuits and ADC's to be capable of operating at a supply voltage of 1.5 V and below in the near future. However, designing ADC's for low supply voltage is difficult. In this paper, a 1-V, 8-bit, 50-kS/s successive approximation ADC implemented in a standard 1.2-μm CMOS process is presented. A new biasing scheme and current-mode approaches have been employed to design a low-voltage S/H, DAC, and latched comparator. The ADC consumes less than 0.34 mW and has an effective number of bits (ENOB) of 7.9 for a 1-kHz input with close to rail-to-rail signal swing. This design demonstrates that low-voltage ADC with medium accuracy can be realized without requiring special enhancements to CMOS technology.

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