Q2. Design a single-bit wide, 64-bit long shift register in Verilog HDL. You should provide the top-level behavioral design, structural design and dataflow design, Verilog HDL, test strategy and the simulation waveforms.

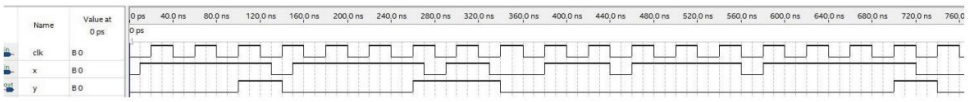
Q3. Design {c,s} = w + x; where [3:0] w, x;. Provide the data flow, behavioral, and structural description along with the test bench. Ensure that the appropriate clock values are given and mention them in the report along with the Timing Diagram and Truth Table.

Q4. Design a circuit for arithmetic subtraction option using XOR and Full Adder Module (Combine the gates to form the Full Adder Module). Provide full description of the subtraction circuit.

Q5. Using the knowledge of Verilog Design the First In First Out FIFO and Moore Sequence Detector.

Q6. Design a sequential circuit using Finite State Machine (FSM) approach that provides a HIGH (1) on output “y”, when either the pattern “1110” or “1101” has been received on the input. Once the final bit of the of the desired sequence has been received the output should go HIGH on the same clock pulse. Utilizing as few states as possible (K-map minimization), provide the state transition table, state transition diagram, next state equations, output equations and design of the sequential circuit.

Q7. Using Finite State Machine (FSM) design a Moore machine that provides a HIGH (1) on output “y”, when three consecutive input (x) “1’s” have been received as the input. Once the 5 third “1” of the sequence has been received the output should go HIGH on the same clock pulse. A typical input, output pattern is shown below:



Provide the state transition diagram, state transition table before showing the Verilog HDL code, test strategy and the captured simulation waveforms.

Q8. Design a Mealy Machine sequence detector. Provide module diagram, logic and the explanation. Concentrate your explanation based on the sequence for which you have designed your system. Provide full justification.