Low-power, Folded Cascode Near Rail-to-Rail OTA for Moderate Frequency Signal Processing

Tripurari Sharan
ECE Department of North Eastern Regional Institute of Science & Technology, Nirjuli, Arunachal Pradesh, 791109, India
tsh1962mzp@gmail.com

Nipu Kumar Nath
ECE Department of North Eastern Regional Institute of Science & Technology, Nirjuli, Arunachal Pradesh, 791109, India
nipukumarn@gmail.com

***Abstract*—This paper presents a gate-driven, folded-cascode operational transconductance amplifier (FCOTA), operating in strong inversion region. The input core utilizes two complementary PMOS and NMOS input pairs to ensure rail-to-rail input common mode range (ICMR). The cascoded load structure at output port performs the job of current summer and provides enhanced gain due to high output impedance for FCOTA. The proposed OTA has been employed to implement universal biquadratic low-pass, high-pass, band-pass and notch transfer functions, simultaneously available at different nodes of the filter. The proposed FCOTA used dual supply voltage of ± 0.9V and dissipates around 93.6 µW power and provides 80.24 dB open loop gain and gain bandwidth (GBW) of 6.03 MHz. The Cadence VIRTUOSO environment using UMC 0.18 µm CMOS process technology has been used to simulate the proposed circuit.**

Keywords— Operational transconductance amplifier (OTA); gate-driven; folded cascode; rail-to-rail; input common mode range; Biquadratic G_m-C filter.

I. INTRODUCTION

Operational Transconductance Amplifier (OTA) is an important building block frequently used in analog signal processing systems design. Out of many OTA structures the folded-cascode structure is very popular owing to its high output swing as compared to telescopic counterpart [1], [2]. In usual telescopic cascode same types of transistors are used in differential pair as well as its cascode stack, whereas folded-cascode uses complementary transistors in differential pair and its cascode load. The FCOTA offers good input common mode range, voltage gain equivalent to two-stage structure [3]–[9]. It does not need additional compensation capacitor, so it is self-compensating and offers increased speed. This structure needs multiple current sources which increases its power consumption. However, its self-load-compensated property make its power consumption comparable to two-stage frequency compensated structure [10]–[13]. The input core of amplifier generally utilizes either NMOS or PMOS pair [14]. The NMOS input pair ensure the input common mode range close to positive supply voltage (V_{DD}) whereas its negative input range is limited to $V_{ic,\min} = (V_{GSN} + V_{DSN})$ where V_{GSN} is the gate to source voltage of NMOS input pair and V_{DSN} is the voltage requirement for NMOS tail MOSFET for its saturation region operation. The reduced negative ICMR can be enhanced by using a PMOS input pair, but its positive input common mode range is limited to $V_{ic\max} = (V_{DD} - V_{SGP} - V_{SDP})$, where V_{SGP} and V_{SDP} are the source to gate voltage of PMOS input pair and source to drain voltage of its tail current PMOS [15]. Thus to ensure rail-to-rail ICMR, both types of NMOS and PMOS input pairs have been proposed [14], [15]. One difficulty with dual input pairs occurs due to different value of transconductance(s) for two cases [6]. In one case either PMOS input pair or NMOS input pair is ON when ICMR is very close to V_{DD} or V_{SS}, respectively. In this case, overall transconductance is either equivalent to g_{mN} or g_{mP} where the g_{mN} and g_{mP} are the transconductance(s) of NMOS and PMOS input pair, respectively. In second case both the pairs are ON when ICMR is in the middle of power supply rails and overall transconductance (G_m) increases to sum of NMOS and PMOS transconductance(s), i.e., $G_m = (g_{mN} + g_{mP})$ [14].

In this work a single-ended output folded cascade OTA is proposed which uses two complementary input differential pairs and two common gate amplifiers comprised of two-diode connected structures, which have ensured low-internal impedance node in cascode load section. Thus, this two-stage FCOTA has only one high impedance node at its single ended output port. This enables its usability in the design of G_m-C filters requiring single ended output structure [17]. The two-stage FC-OTA structure is self-load compensated and don't need compensation capacitor, so it consumes less quiescent power than multi-stage FC-OTAs reported in [18].

The remaining paper has been organized as follows. The design of the proposed transconductor is presented in Section II. The simulation results of the proposed OTA are discussed in Section III, Section IV describes its application as universal biquadratic G_m-C filter along with its results and finally Section V concludes the paper.

II. PROPOSED FCOTA CIRCUIT

The Fig. 1 shows a folded cascode OTA which utilize two complementary input pairs to ensure rail-to-rail ICMR. The p-channel MOSFET pair (MP_1, MP_2) extends ICMR down to negative supply whereas the n-channel input pair comprised of MOSFET pair (MN_1, MN_2) extends the ICMR close to positive rail supply. The circuit section MP_8, MN_8 and resistor R_B of value 53 kΩ generates bias current I_{Bias} around 12 µA which is copied and routed to different

978-1-5090-5620-0/17/$31.00 ©2017 IEEE

sections via the current mirrors comprised of MP_3, MP_9 and MN_3, MN_9 to generate the tail currents for PMOS and NMOS input pairs, respectively. The tail currents of NMOS and PMOS both of input pairs are set to 12 µA to optimize power dissipation and required unity gain frequency (UGF) as a design trade-off. The current summer section utilizes all diode connected MOSFETs as fully differential to single ended converter which avoids the need of additional reference voltage to bias the gates of cascode structures and reduce power consumption.

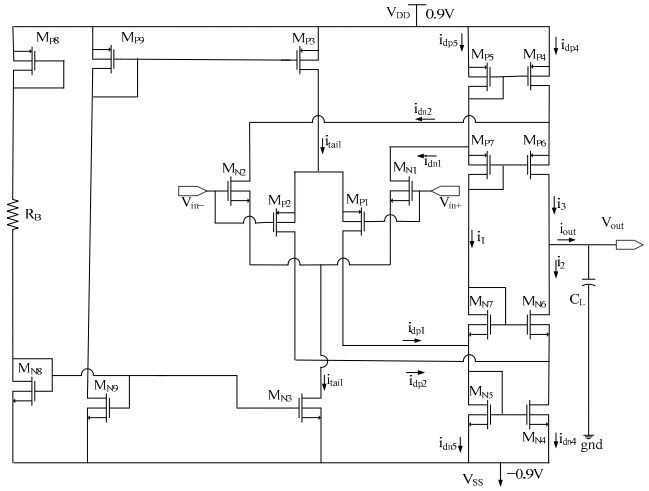

Fig. 1. The rail-to-rail input swing single ended FC-OTA.

Performance equations:

The general circuit analysis for circuit shown in Fig. 1 provides the output current (i_{out}) given by

$$i_{out} = i_3 - i_2 = (i_{dp2} - i_{dp1}) + (i_{dn2} - i_{dn1}) \quad (1)$$

where $(i_{dp2} - i_{dp1})$ is the differential output current of the PMOS pair which is equal to $g_{mP}(v_{in}^{+} - v_{in}^{-})$ similarly, the differential current $(i_{dn2} - i_{dn1}) = g_{mN}(v_{in}^{+} - v_{in}^{-})$ is generated by NMOS pair. The small signal output current i_{out} flows through the equivalent impedance (R_{out}) seen at the common drain of MP_6 and MN_6 (see Fig. 1). By substituting the small signal differential input voltage $v_{in} = \left(v_{in}^{+} - v_{in}^{-}\right)$, the output voltage $v_{out} = (g_{mN} + g_{mP}) R_{out} v_{in}$ with $R_{Out} = R_{ON} \| R_{OP}$ where $R_{OP} \cong g_{mP6} r_{oP6} (r_{oP4} \| r_{oN2})$ and $R_{ON} \cong g_{mN6} r_{oN6} (r_{oN4} \| r_{oP2})$ where g_{mi} and r_{oi} are the transconductance and output impedance of cascode load sections and i stands for the name of the concerned MOSFET. So, the open loop voltage gain of this FCOTA is $(g_{mN} + g_{mP}) R_{out}$.

III. Simulation Results

The aspect ratio of the MOSFETs used in this FCOTA is shown in Table I. The various performances of the proposed FCOTA have been simulated in Cadence Virtuoso

TABLE I
ASPECT RATIO OF MOSFET USED IN FCOTA

MOSFET	W(µm)	L(µm)
M_{N1}, M_{N2}, M_{P3}, M_{P9}, M_{P8}	10	1
M_{P1}, M_{P2}, M_{P6}, M_{P7}	20	1
M_{N4}, M_{N5},	30	2
M_{P4}, M_{P5}	80	1
M_{N8}, M_{N9}	5	1
M_{N3}	5.5	1
M_{N6}, M_{N7}	10	2

environment using 180 nm standard n-tub CMOS process technology in UMC library file. This OTA is biased in strong inversion region setting a quiescent tail current of 12 µA for both the input pairs.

The open loop AC response simulation results for this FCOTA with load capacitor C_L of 5 pF is shown in Fig. 2. It has offered open loop gain of 80.24 dB and gain bandwidth (GBW) of 6.03 MHz. Its AC response ensured phase margin (PM) of 73.8, which confirms its stable operation. There exists trade-off between high frequency performance and power dissipation, so GBW, slew rate (SR) and tail current, I_{Bias} should be set as per the need to optimize total current as well as total quiescent power consumption for a given power budget.

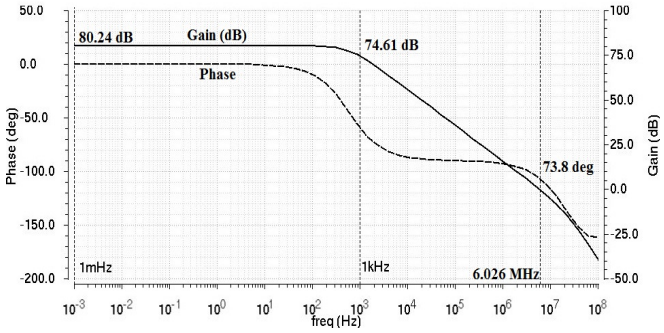

Fig. 2. AC response showing gain (solid-trace) and phase (dashed-trace).

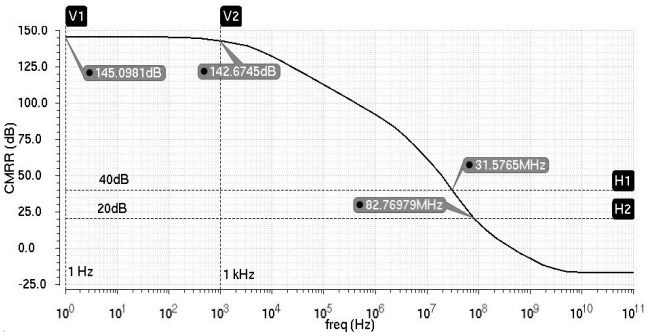

Fig. 3.AC analysis response showing CMRR.

The Fig. 3 shows CMRR vs frequency plot of this FCOTA. It provided 145 dB CMRR at 1 Hz frequency and 142.67 dB CMRR at 1 kHz frequency. The CMRR remains

40 dB and 20 dB up to 31.6 MHz and 82.7 MHz, respectively. The folded cascode load enhanced its output impedance as well as CMRR of this circuit.

The power supply rejection ratio (PSRR) of FCOTA should be high enough to minimize the effect of on-chip noise coupled to power supply rails. The simulation result depicts that this FCOTA has ensured PSRRs of 87.27 dB, 82.23 dB, 40 dB and 20 dB at frequencies of 1 Hz, 1 kHz, 9.65 MHz and 46.3 MHz, respectively. The PSRR generally approaches 0 dB at unity gain frequency however, this OTA has ensured PSRR of 40 dB and 20 dB up to 9.65 MHz and 46.3 MHz frequencies, respectively as shown in Fig. 4.

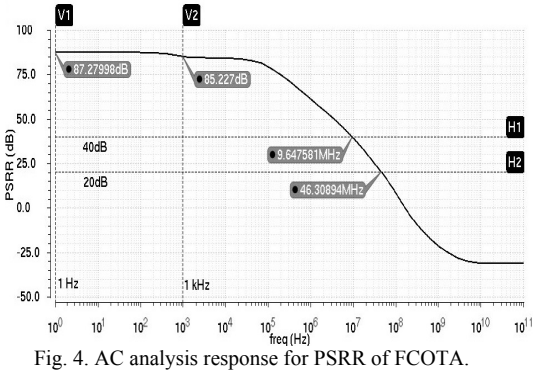

Fig. 4. AC analysis response for PSRR of FCOTA.

The noise referred to input ports of the OTA should be minimized for its good noise immunity. The noise analysis in open loop AC response set up has been performed and the simulation result of input referred noise (inoise) at gate terminal is shown in Fig. 5. This OTA generates low inoise of 99 nV/Sqrt Hz and 21 nV/sqrt Hz at 1 kHz and 100 kHz frequencies, respectively.

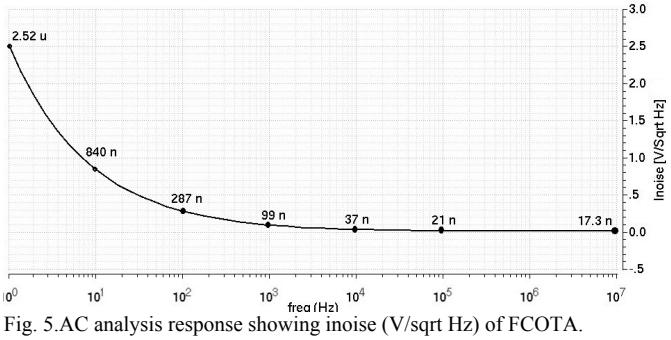

Fig. 5.AC analysis response showing inoise (V/sqrt Hz) of FCOTA.

The positive and negative slew rates have been evaluated in unity gain configuration of the FCOTA using 1.8 V_{PP} pulse of 10 kHz frequency. The pulse transient analysis for the proposed OTA has offered the positive and negative slew rates of 3.42 V/µs and 3.56 V/µs as shown in Fig. 6.

The linearity range has been investigated by performing the DC sweep (− 0.9 V-to-0.9 V) analysis in unity gain configuration for two-complementary input pairs based FCOTA. The input and output voltage closely tracks each other for ICMR of nearly −790 mV-to-740 mV as depicted in Fig. 7.

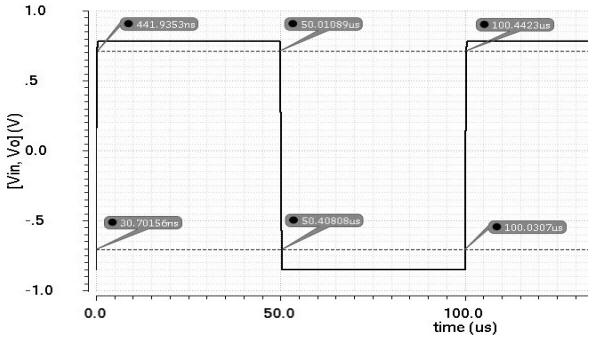

Fig. 6. Pulse transient response of the FCOTA.

It ensured the ICMR range of 1.53 V out of 1.8 V supply. The Fig. 8 shows the DC sweep result and ICMR for single NMOS input pair based FCOTA. The negative ICMR has been reduced from −790 mV to −600 mV. The Fig. 9 shows the DC sweep result and ICMR for single PMOS input pair based FCOTA. The positive ICMR has been reduced from 740 mV to 500 mV. Thus, the complementary input pairs based FCOTA structure has offered very near rail-to-rail ICMR.

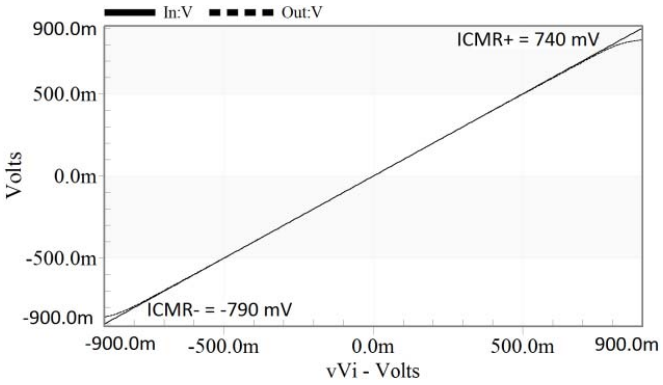

Fig. 7. DC sweep of V_{in} and V_{Out} for NMOS-PMOS input pair FCOTA.

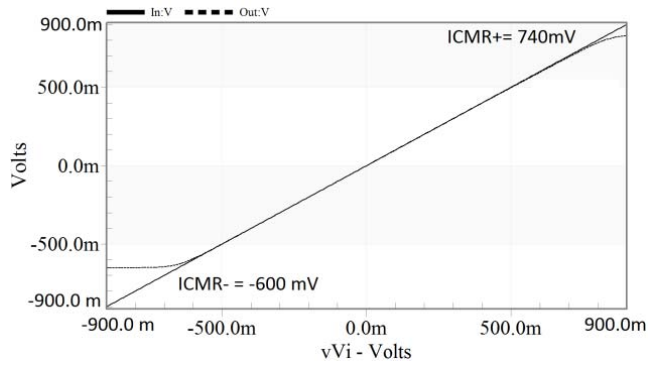

Fig. 8. DC sweep of V_{in} and V_{Out} for NMOS input pair FCOTA.

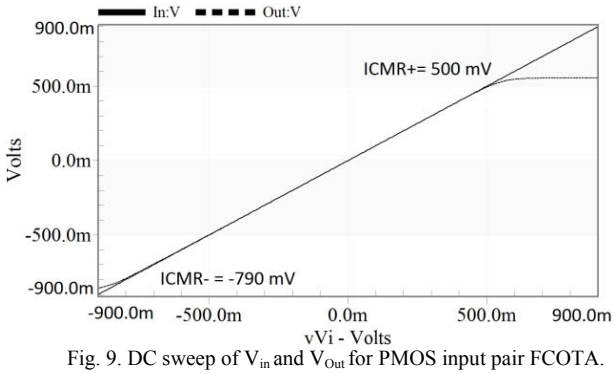

Fig. 9. DC sweep of V_{in} and V_{Out} for PMOS input pair FCOTA.

The THD for the FCOTA has been measured in unity gain configuration using a 100 Hz sine wave of varying peak values in the range of 100 mV to 1.6 V. The transient response of FCOTA for sine wave input of 1.4 V_{PP} is shown in the Fig. 10. The THD of the OTA for different peak to peak input voltage have been listed in the Table II.

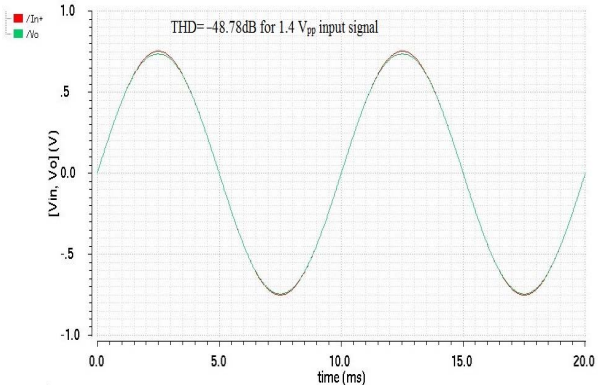

Fig. 10. Transient analysis response in unity gain configuration of the FCOTA for 1.5 V_{PP} input at 100 Hz frequency.

TABLE II
THD FOR DIFFERENT PEAK-TO-PEAK INPUT SIGNAL

Peak-to-peak input voltages	THD (dB)
100 mV_{pp}	−64.61
500 mV_{pp}	−64.64
600 mV_{pp}	−65.05
800 mV_{pp}	− 63.48
1.4 V_{pp}	− 48.78
1.5 V_{pp}	− 44.4
1.6 V_{pp}	− 37.08

The Table III and Fig. 11 depict the corner case results which show effect of all five device corners on the AC analysis. It ensures very slight deviation in Gain, unity gain frequency (UGF) and PM for different device corners. This confirms stable and robust design of FCOTA against process mismatch effects.

TABLE-III
CORNER CASE SIMULATION RESULT OF FCOTA

Corner	Type	Gain(dB) at 1 mHz	Gain (dB) at 1 kHz	UGF (MHz)	PM (deg)
nom	TT	80.24	74.61	6.03	73.8
C_0	SS	81.98	74.24	5.21	67.87
C_1	FF	77.88	74.27	6.98	77.87
C_2	SF	80.16	74.61	6.31	74.37
C_3	FS	80.22	74.59	6.24	73.66

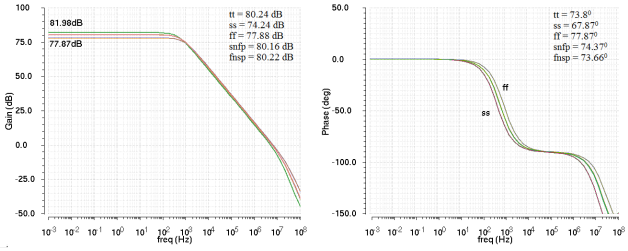

Fig. 11. Corner analysis of FCOTA for gain and phase margin.

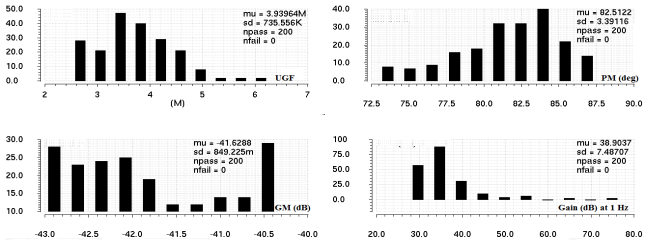

Fig. 12. Monte Carlo simulation under random process and mismatch and generated histograms for UGF, PM, GM, Gain of FCOTA.

The Monte Carlo simulations for proposed OTA has also been performed using number of occurrences of 200 with expression of open loop gain, UGF, PM, gain-margin (GM) as depicted in Fig. 12 and Table IV.

TABLE IV
MIN., MAX., MEAN, STANDARD DEVIATION VALUES OF VARIOUS AC PERFORMANCES FOR MONTE CARLO SIMULATION

Parameter	Minimum value	Maximum value	Mean Value	Standard Deviation
GM	40.17 dB	42.8 dB	41.6	849m
Gain (dB) at 1Hz	30 dB	80.09 dB	39	7.5
PM (deg.)	73.67	88.42	82.5	3.4
UGF (MHz)	2.69	6.51	3.94	0.74

IV. APPLICATION IN GM-C FILTERS

The proposed OTA has been utilized to design a universal biquadratic G_m–C filter which generates low-pass, high-pass, band-pass and band-stop functions simultaneously at three different nodes as shown in the Fig. 13. The V_i denotes the input signal and V_{LP}, V_{HP}, V_{BP} and V_N presents low-pass, high-pass, band-pass and band-stop (notch) filter

responses, respectively. The filter is designed for a second order system comprised of nine-identical G_m cells. This filter consists of two-G_m-C integrators and one OTA based adder. The G_{m1} and C_1 performs as an inverting integrator whereas G_{m2} and C_2 works as non-inverting integrator. The G_{m5} cell acts as a negative grounded resistor offering resistance of ($-1/G_{m5}$ ohm). This filter consumed a total power of 720 µW. The circuit shown in Fig. 13 has realized all five biquadratic filter functions.

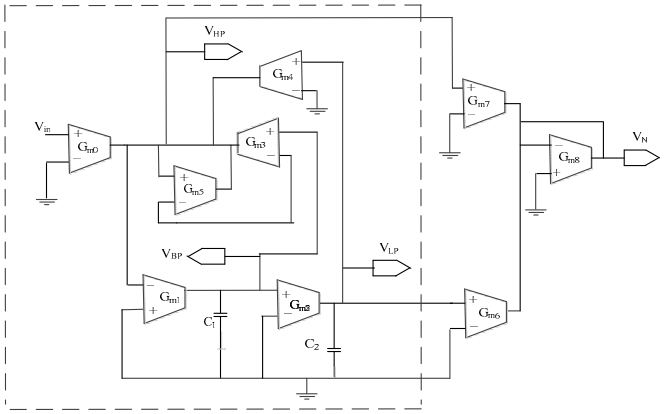

Fig. 13. Biquadratic G_m-C filter shown in dashed boundary containing six-OTA cells and two capacitors as adopted from [16], realizes low-pass, high-pass and band pass filter function, and proposed notch filter, shown outside the dashed-boundary, utilizes 3-OTAs to generate 2-input inverting summer which sum low-pass and high-pass functions to yields notch filter response.

Transfer characteristics of the filter:

This biquadratic filter circuit on routine analysis provides low-pass, high-pass, band-pass and notch transfer functions as shown in (2)–(5) for all identical G_m cells. Refer [16] for detailed analysis.

$$\frac{V_{LP}(s)}{V_i(s)} = \frac{-\frac{G_m^{\,2}}{C_1C_2}}{s^2 + s\frac{G_m}{C_1} + \frac{G_m^{\,2}}{C_1C_2}} \tag{2}$$

$$\frac{V_{HP}(s)}{V_i(s)} = \frac{s^2}{s^2 + s\frac{G_m}{C_1} + \frac{G_m^{\,2}}{C_1C_2}} \tag{3}$$

$$\frac{V_{BP}(s)}{V_i(s)} = \frac{\frac{-sG_m}{C_1}}{s^2 + s\frac{G_m}{C_1} + \frac{G_m^{\,2}}{C_1C_2}} \tag{4}$$

$$\frac{V_N(s)}{V_{IN}(s)} = \frac{s^2 + \frac{G_m^{\,2}}{C_1C_2}}{s^2 + s(\frac{G_m}{C_1}) + \frac{G_m^{\,2}}{C_1C_1}} \tag{5}$$

The standard second order all pass biquadratic filter function is given by

$$\frac{V_{AP}(s)}{V_i(s)} = \frac{s^2 - \frac{\omega_0}{Q}s + \omega_0^{\,2}}{s^2 + s\frac{\omega_0}{Q} + \omega_0^{\,2}} \tag{6}$$

Comparing the denominators of (5), (6) the central frequency (ω_0) and quality-factor (Q) of the filter are $\omega_0 = G_m/\sqrt{C_1C_2}$ and $Q = \sqrt{C_1C_2}$.

The Fig. 14 shows low-pass, high-pass and band-pass filter functions for filter capacitors $C_1 = C_2 = 1$ nF.

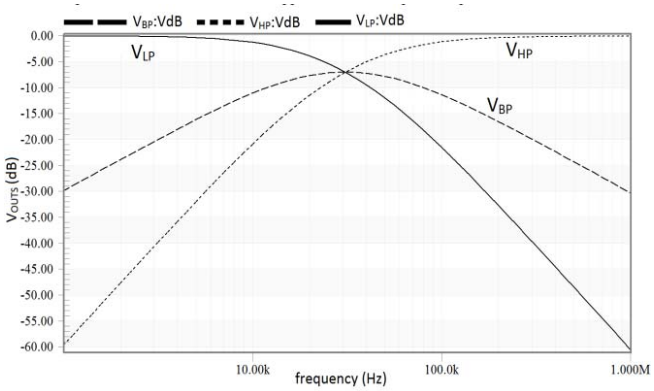

Fig.14.Biquadratic filter functions showing LP, HP, BP responses.

Fig. 15 shows the notch filter response when filter capacitors C_1 and C_2 have been set to 1 nF. The calculated notch frequency $f_N = \sqrt{}(f_H \cdot f_L) = 5.465$ kHz. The f_N value from this plot is found to be 5.6 kHz. Table V summarizes overall results of this biquadratic filter.

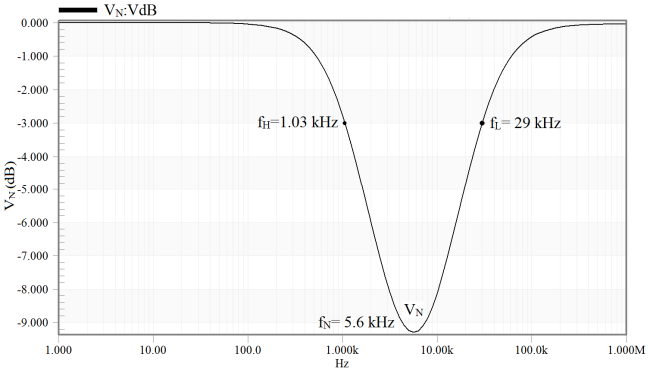

Fig. 15. Notch filter response for $C_1 = C_2 = 1$ nF.

TABLE V

PERFORMANCE RESULT OF BIQUADRATIC FILTER USING PROPOSED OTA.

Types of filter output	Lower cut-off frequency (f_L) kHz	Higher cut-off frequency (f_H) kHz	Mid-point frequency (f_0) kHz
LP	18.9	–	–
HP	–	54	–
BP	12.2	76.9	30.2
Notch	29	1.03	5.6

The performance comparison of some FC-OTA circuits has been performed using the Figure of Merit (*FoM*) given by

$$FoM = \frac{Gain(dB)\,GBW(MHz)\,C_L(pF)}{Power(\mu W)} \quad (7)$$

TABLE VI

PERFORMANCE COMPARISION OF PROPOSED FCOTA WITH OTHER FCOTAS PROPOSED IN [8], [10], [17].

Parameters	**This work**	**[8]**	**[10]**	**[17]**
Supply voltage	± 0.9	2.5	± 2	1.8
CMOS process (nm)	180	350	350	180
Gain (dB)	80.24	> 80	77.53	60.9
GBW (MHz)	6.03	200	430	134.2
Phase margin (deg)	73.8	>50	58	70.6
CMRR (dB)	145.09	>70	114	–
PSRR (dB)	86.29	>70	46.5	–
Slew rate (V/µs)	3.67	100	196	94.1
Power (µW)	93.6	<3000	660	1440
I_{Bias}(µA)	11.05	–	55	–
THD for 1.4 V_{pp} (dB)	−48.78	–	–	–
Inoise (µV/Sqrt Hz)	2.52	–	–	–
C_L (pF)	5	10	0.1	5.6
FoM	25.84	16	5.05	31.78

Table VI shows the performance comparison and this FCOTA has provided maximum Gain, PM, CMRR, PSRR among others. Its *FoM* is also maximum among others except [17]. The FCOTA proposed in [17] provides more *FoM* at the cost of increased power dissipation.

V. CONCLUSIONS

In this paper a moderate power gate-driven single-stage FCOTA operating in strong inversion region has been presented. This circuit utilizes two complementary input pairs to ensure very near rail-to-rail input common mode range. The folded cascode structure has ensured reasonable performances at moderate power consumption of 93.6 µW. This FCOTA has ensured the gain of 80.24 dB, GBW of 6 MHz, PM of 73.8^0 and slew rate of 3.67 V/µs. It has provided high CMRR and PSRR of 145 dB and 86.3 dB, respectively. This FCOTA cell has also been utilized to design a second order biquadratic G_m-C filter suitable for low-power audio and sub-video signal processing.

Acknowledgement

This work has been performed in Cadence Spectre environment and UMC library file of 0.18 µm standard n-tub CMOS process technology, utilizing the resources of VLSI laboratories of ECE and EE departments, developed under TEQIP-II project funded by Ministry of Communication and Information Technology Government of India at NERIST, Nirjuli, Arunachal Pradesh India.

REFERENCES

[1] Z. Kun, W. Di, L. Zhangfa, "A High-performance Folded Cascode Amplifier," *International Conference on Computer and Automation Engineering, IPCSIT, IACSIT Press, Singapore*, vol. 44, 2012, pp. 41–44.

[2] P. Allen and D. Holberg, *CMOS Analog Circuit Design*, 3rd ed. Oxford, U.K.: Oxford Univ. Press, 2011, pp. 302–306.

[3] Sakshi Dhuware, Mohammed Arif, "Low Voltage, Low Power Rail to Rail Operational Transconductance Amplifier with Enhance Gain and Slew Rate,"*International Journal of Engineering Research and General Science* Vol. 2, Issue 5, 2014, pp. 616–621.

[4] Giuseppe Ferri, Vincenzo Stornelli, Angelo Celeste, "Integrated Rail-to-Rail Low-Voltage Low-Power Enhanced DC-Gain Fully Differential Operational Transconductance Amplifier," *ETRI Journal*, Vol. 29, 2007, pp.785–793.

[5] Xiao Zhao, Huajun Fang, Jun Xu, "A Low Power Constant-G_m Rail-to-Rail Operational Transconductance Amplifier by Recycling Current," *IEEE*, DOI**:**10.1109/EDSSC.2011.6117572.

[6] M. Akbari, S. Biabanifard, S. Asadi, M. C. E. Yagoub, "High perform–ance folded cascode OTA using positive feedback and recycling structure," *Analog Integr Circ Sig Process, Springer* 2015, pp. 217–227.

[7] Vivek kumar, Kamal K Kashyap, "A simple low power OTA based circuitry for constant-g_m rail-to-rail operation," *IEEE*, DOI:10.1109/ICSPCT.2014.6885004, pp. 151–157.

[8] K.B. Maji, R. Kar, D. Mandal, S.P. Ghoshal, "An evolutionary approac -h based design automation of low power Two-Stage Comparator and Folded Cascode OTA CMOS", *Int. J Electron. Commun. (AEU)*, 2016, pp. 398–408.

[9] Omar Abdelfattah, "An ultra-low-voltage CMOS process-insensitive self-biased OTA with rail to rail input range," *IEEE transactions on circuits and system-I*, 2015, Vol. 62, No. 10, pp. 2380–2390.

[10] H. Daoud Dammak, S. Bensalem, S. Zouari, M. Loulou, "Design of Folded Cascode OTA in Different Regions of Operation through g_m/I_D Methodology," *International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering*, Vol. 2, No. 9, 2008, pp. 1741–1746.

[11] Y.L. Li, K.F. Han, X. Tan, N. Yan and H. Min, "Transconductance en-hancement method for operational transconductance amplifiers," *ELECTRONICS LETTERS*,Vol. 46, No. 19,DOI:10.1049/el.2010.1575.

[12] R. L. Geiger, E. Sánchez-Sinencio, "Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial," IEEE *Circuits and Devices Magazine*, Vol. 1, March 1985, pp. 20–32.

[13] Montree Kumngern , Boonying Knobnob, Kobchai Dejhan, "Electronic -ally tunable high-input impedance voltage-mode universal biquadratic filter based on simple CMOS OTAs,"*Int. J. Electron. Commun. (AEU)*, 2010, pp. 934–939.

[14] Rasoul Dehghani, *Design of CMOS Operational Amplifiers*,Artech House, Boston, London, 2013, pp. 86–105.

[15] R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*, IEEE press series on microelectronics systems.

[16] Tahira Parveen, *A textbook of Operational Transconductance Amplifier and Analog Integrated Circuits*,I. K. International Pvt. Ltd, pp. 171–173, Chap. 7.

[17] Assaad R, Silva-Martinez J., "The recycling folded cascode: a general enhancementof the folded cascode amplifier,"*IEEE J Solid-State Circuits* 2009, vol. 44, pp. 2535–2542.

[18] A.D. Grasso, D. Marano, G. Palumbo, S. Pennisi, "Analytical comparison of reverse nested Miller frequency compensation techniques," Int. J. Circ. Theor. Appl. vol. 38, pp. 709-737, 2010.