3.3kW CLLC Converter with Synchronous Rectification for Plug-in Electric Vehicles

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***Abstract*— This paper presents an innovative technique for synchronous rectification in the bidirectional CLLC converter with the integrated transformer for plug-in electric vehicle (EV) applications. To improve the efficiency and power density, the integrated transformer is introduced and simulated using Finite Element Analysis (FEA) method. In addition, synchronous rectification method is implemented by controlling the turn-on and turn-off timings based on the phase difference between resonant currents of primary and secondary sides. Furthermore, a simplified closed loop design is discussed and implemented on a digital signal processor (TMS320F28335). The effectiveness of the control loop is verified through the experimental results. A 3.3*kW* proof-of-concept prototype is built with power density of 1*kW/L*, a gravimetric power density of 0.9*kW/kg* and peak efficiency of 97.5%.**

***Index Terms*—Bidirectional converter, electric vehicles (EVs), integrated transformer, phase control**.

I. Introduction

In selection of the DC/DC stage topology for traditional onboard chargers, LLC resonant converter is a suitable candidate for unidirectional grid-to-vehicle (G2V) chargers due to its high efficiency and wide output range [1-2]. Moreover, vehicle-to-grid (V2G) has drawn significant attention due to the flexibility for feeding electricity back into the grid for load leveling purposes [3]. Thus, CLLC and Dual Active Bridge (DAB) are examined as two most commonly used DC/DC converter topologies for bidirectional EV charger applications [4-6]. However, the soft switching region of a conventional DAB converter is only limited to a narrow output voltage range [7]. Therefore, researchers have proposed an improved DAB control strategy in [8] to improve efficiency, through implementing a modified modulation index in one of the two bridge legs and a phase shift between the primary and secondary voltages. In comparison to the DAB, a bidirectional CLLC converter can be operated in a wide output range [9]. Many recent studies have been conducted towards this topology. Research in [10] proposes a maximum efficiency tracking methodology for a CLLC converter; however, it does not present any experimental results to solidify its claim. In [11], the design criteria are presented for a CLLC converter to get an optimized solution. However, the lack of synchronous rectification in secondary side results in high conduction loss. In [12], coupling capacitors are implemented to eliminate the circulating loss in the resonant tank for wireless charging applications. Nevertheless, none of the aforementioned studies provides any details on the closed-loop design and system stability analyses.

To overcome the aforementioned considerations, this paper introduces an innovative technique for achieving synchronous rectification in a bidirectional 3.3kW CLLC converter for onboard charger applications. In addition, the paper presents the detailed design and analyses to meet the requirement of wide range output voltage and to ensure soft-switching for efficiency improvement. Moreover, to achieve the constant voltage (CV) charging for battery, a PI-based control strategy is implemented in digital domain. This manuscript is organized as follows: The CLLC topology and its voltage gain characteristics are analyzed in Section II. Design methodology of the power stage is discussed in Section III. The Section IV presents the design methodology of control stage including frequency modulation and the proposed synchronous rectification approach. The simulation and experimental results are presented in Section V. Section VI puts forward the conclusions with relevant discussions.

II. DC Characteristics of CLLC Converter

Fig. 1 shows the topology of a bidirectional half-bridge CLLC resonant converter and the power flow directions of charging mode (G2V) and discharging mode (V2G). The topology utilizes an integrated transformer for offering galvanic isolation between the primary and secondary sides. L_m, L_{r1} and L_{r2} are the magnetizing inductance, primary side leakage inductance and secondary side leakage of the transformer, respectively. C_1 and C_2 play the role of the half bridge DC capacitors and the resonant capacitors, simultaneously.

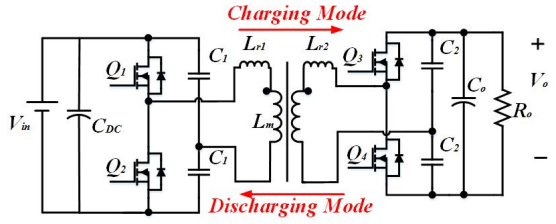


Fig. 1. Topology of half-bridge CLLC converter

A. Gain Analysis

(i) Equivalent Circuit in G2V

Equivalent circuit of a half-bridge CLLC converter in charging mode is shown in Fig. 2. Assume that 'n' denotes the turns ratio of the transformer. Using First Harmonic Approximation (FHA), equivalent load resistance ($R_{e,c}$) can be expressed as follows [9].

$$R_{e,c} = \frac{2n^2}{\pi^2} R_o \tag{1}$$

where, R_o is the load resistance in G2V mode.

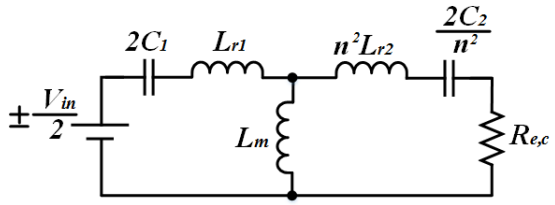


Fig. 2. Equivalent circuit of the CLLC converter in charging mode.

All the equivalent resonant parameters in charging mode can be referred to the primary side as follows.

$$L'_{r2} = n^2 L_{r2},\ C_{r1} = 2C_1,\ C_{r2} = \frac{2C_2}{n^2} \tag{2}$$

In addition, the normalized frequency and quality factor are defined as follows.

$$\omega = \frac{\omega_s}{\omega_r},\ Q_c = \frac{\sqrt{\frac{L_{r1}}{C_{r1}}}}{R_{e,c}},\ \omega_r = \frac{1}{\sqrt{L_{r1}C_{r1}}} \tag{3}$$

where, ω_r and ω_s denote the resonant frequency and the switching frequency, respectively. ω is the normalized frequency and Q_c is the quality factor in charging mode.

(ii) Equivalent Circuit in V2G

Equivalent circuit of the half-bridge CLLC converter in the discharging mode is shown in Fig. 3. Similar to (1), equivalent load resistance ($R_{e,r}$) in the discharging mode can be modeled as (4).

$$R_{e,r} = \frac{2}{\pi^2 n^2} R'_o \tag{4}$$

where R'_o is the load resistance in V2G mode.

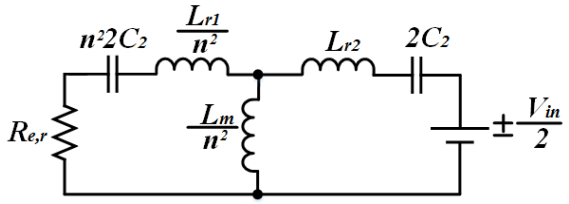


Fig. 3. Equivalent circuit of CLLC in discharging mode.

Similarly, all the equivalent resonant parameters in discharging mode are derived as (5).

$$\begin{cases} L'_{r1} = \frac{L_{r1}}{n^2},\ C_{r1} = \frac{2C_1}{n^2},\ C_{r2} = 2C_2 \\ \omega_r = \frac{1}{\sqrt{L_{r2}C_{r2}}},\ Q_r = \frac{\sqrt{\frac{L_{r2}}{C_{r2}}}}{R_{e,r}},\ L'_m = \frac{L_m}{n^2} \end{cases} \tag{5}$$

where, Q_r is the quality factor in the discharging mode.

(iii) Gain Curve of G2V

For G2V mode, the general transfer function $H(j\omega)$ can be determined by analyzing Fig. (2) and expressed as follows.

$$H(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{1}{n}\frac{R_{e,c}}{R_2}\frac{R_2 // j\omega L_m}{j\omega L_{r1} + \frac{1}{j\omega 2C_1} + R_2 // j\omega L_m} \tag{6}$$

where,

$$R_2 = R_{e,c} + j\omega n^2 L_{r2} + \frac{1}{j\omega\frac{2C_2}{n^2}} \tag{7}$$

The gain function of CLLC converter $G_{G2V}(\omega)$ can be derived from (6) as follows.

$$G_{G2V}(\omega) = |H(j\omega)| = \frac{1}{n}\frac{1}{\sqrt{\left(\frac{1}{k} - \frac{1}{k\omega^2} + 1\right)^2 + \left[\frac{1}{\omega}\left(\frac{a}{k} + \frac{1}{kb} + \frac{1}{b} + 1\right)Q_c - \omega\left(\frac{a}{k} + a + 1\right)Q_c - \frac{Q_c}{kb\omega^3}\right]^2}} \tag{8}$$

where, $k = \frac{L_m}{L_{r1}}, a = \frac{n^2 L_{r2}}{L_{r1}},\ b = \frac{2C_2}{n^2 C_1}$ (9)

Fig. 4 shows the gain curves at different loads based on the derivation of gain function $G_{G2V}(\omega)$. According to this figure, the peak of the gain curve reduces when the quality factor decreases, which implies that it tends to enter capacitive region at a lighter load if the switching frequency range is not appropriately designed.

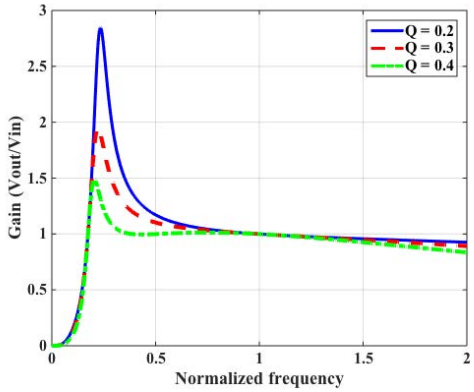


Fig. 4. Gain curves versus normalized frequency with different loads.

B. Primary Side Zero-Voltage-Switching (ZVS) Consideration

ZVS of primary side MOSFETs can be achieved when the slope of the gain curve in Fig. 4 is negative, which is known as inductive region. Another requirement for ZVS is that the magnetizing inductor current must be large enough to fully charge or discharge the MOSFET junction capacitor during dead time. Therefore, L_m should be limited below a maximum limit [9].

$$L_m \le \frac{t_{db}}{8C_S f_{s,max}} \tag{10}$$

Where, t_{db} is the dead time, C_S is the MOSFET junction capacitance and $f_{s,max}$ is the maximum switching frequency.

III. Design Methodology of the Power Stage

A. Design Considerations of Parameters

Resonant frequency f_r is selected 130kHz for G2V mode and 100kHz for V2G mode considering the trade-offs between EMI, efficiency, power density and control

complexity. Reducing resonant frequency would improve efficiency due to the reduced copper and iron losses in the transformer. However, it may potentially cause severe EMI issues and result in degradation of the power density [13].

The input voltage of CLLC converter is 600V. For the CLLC design in this work, the output voltage range is kept at 250V ~ 420V, which aims at charging an EV battery pack. In charging mode, the nominal load is 52Ω with 400V output voltage. Turns ratio of the transformer, n, is designed as 1.5 considering 600V input and 400V output. Based on the turns ratio, gain range is designed to be 0.8 ~ 1.1 and 0.52 ~ 0.98 in charging and discharging modes, respectively, which satisfy the wide range output requirement. In order to reduce the size and weight of magnetic components, leakage inductances of the transformer windings are utilized as resonant inductors, which physically eliminates the resonant inductors. A list of key design parameters for both the charging and discharging modes is summarized in Table 1.

Table 1. Designed parameters for G2V and V2G modes

Parameters	G2V	V2G
Resonant frequency f_r (kHz)	130	100
Gain range	0.8 ~ 1.1	0.52 ~ 0.98
Primary resonant capacitance C_1 (nF)	33	
Secondary resonant capacitance C_2 (nF)	77	
Primary resonant inductance L_{r1} (μH)	21	
Secondary resonant inductance L_{r2} (μH)	19	
Magnetizing inductance L_m (μH)	340	
Turns ratio n	1.5	

Fig. 5 shows the gain curves in both G2V and V2G modes. To ensure gain requirements at different operating points confirming ZVS, the range of switching frequency is selected from 100 kHz to 200 kHz.

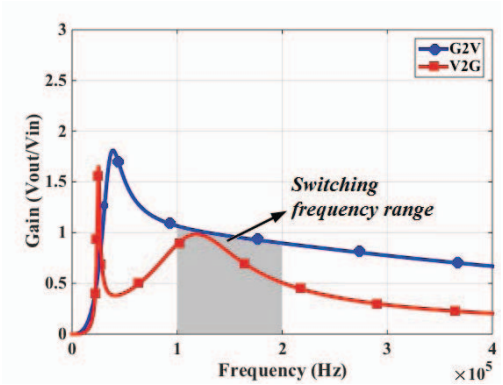


Fig. 5. Designed gain curves versus frequency in G2V and V2G modes.

B. Design of Electromagnetic Integrated Transformer

In order to minimize the core and winding losses and to improve power density, an electromagnetic integrated transformer, shown in Fig. 6 is designed and an airgap is provided to avoid the flux saturation. The resonant inductances are integrated into a gapped transformer with a singular arrangement of primary side and secondary side. Considering the power rating and the flexibility to manage the leakage air gap, E65 core with 3F3 material from Ferroxcube is selected. By increasing winding turns to increase flux density, core loss can be reduced. Thus, the number of turns in the primary and secondary sides are 20 and 15, respectively, considering the trade-offs among window area, turns ratio, power rating and magnetic inductance requirements. Table 2 summarizes several key parameter specifications of the integrated transformer.

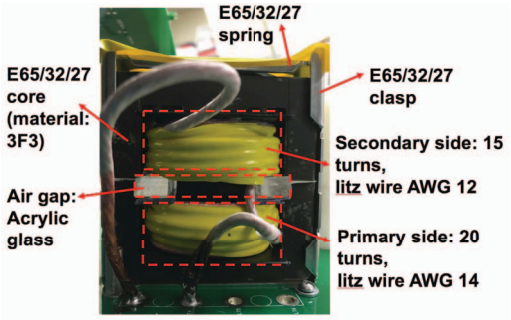


Fig. 6. Photograph of the designed integrated transformer.

Fig. 7 shows the results obtained in finite element analysis (FEA) simulation of the designed integrated transformer in Maxwell. From the simulation, maximum magnetic flux B_{max} is directed along the middle column of the core with a magnitude below saturation flux density level (0.4T). As observed from the thermal monitoring, the air-gap proximity becomes one of the severe hotspots due to the highest magnetic flux passing through it.

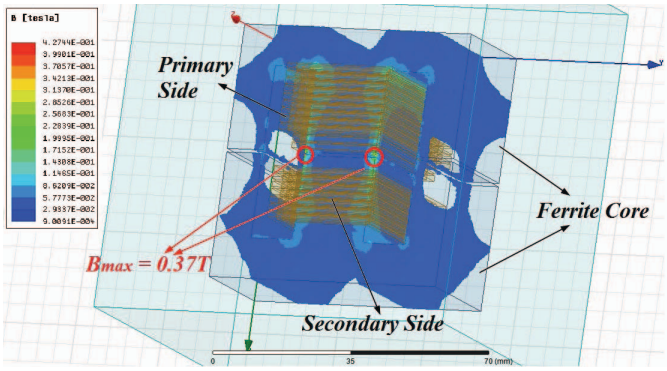


Fig. 7. Simulated magnetic field of the integrated transformer.

Table 2. Parameters of the integrated transformer

Core Size	Core Material	Primary Side Turns	Primary Current	Secondary Side Turns	Secondary Current	Leakage Air Gap	Core Air Gap
E65	3F3	20	13A	15	17A	2.8mm	1mm

IV. Design Methodology of the Control Stage

A. Closed Loop Control Strategy

Frequency modulation as a part of closed loop control is implemented to achieve the constant voltage (CV) charging of the battery, which is demonstrated in the Fig. 9. Voltage control loop is implemented to regulate the output voltage. As indicated by Fig. 8, a general PI compensator is implemented in the feedback loop and the transfer function for a PI compensator is given as (11).

$$C(s) = k_p + \frac{k_i}{s} = k_p\left(\frac{s+z}{s}\right) \quad (11)$$

where, $z = \frac{k_i}{k_p}$ is the zero of controller.

With the increase of k_p, the magnitude response gets a gain offset resulting the zero crossing to be happening at a farther frequency, which increases the bandwidth. This results in a faster dynamic response but may jeopardize stability of the system if the net phase margin degrades.

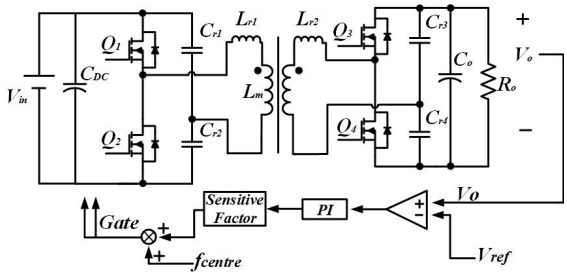


Fig. 8. Voltage control loop structure of the CLLC converter.

As can be seen from Fig. 8, the output voltage PI controller output is multiplied by a sensitive factor to obtain the required change in the switching frequency. At an instant when the output voltage is less than the reference value, the effective switching frequency becomes less than the center frequency to increase the overall gain and vice-versa happens. It is noteworthy to mention that the sensitive factor acts as a common factor to both the proportional and integral gains, which keeps the controller zero location intact. However, the equivalent proportional parameter (k_p) increases with a higher sensitivity factor, which in turn increases the gain-crossover frequency. This helps in achieving a faster dynamic response upon any load/line disturbance at the cost of reduced noise susceptibility, which can be resolved by an appropriate zero selection of the controller.

B. Proposed Synchronous Rectification Method

Due to the characteristics of resonant tank, there exists a phase shift between primary MOSFET gate pulse and resonant current. δ is defined to be the phase delay angle between the primary gate pulse and the secondary gate pulse, which is determined by the resonant network and operating frequency. δ_{max} is the maximum phase angle delay in all the operating conditions, which can be measured experimentally at two boundary operating frequencies without engaging SR. Turn-on of the secondary side switches should be strictly synchronized with the polarity of the secondary resonant current. If the SR timing is not properly set, there will be a circulating current in the secondary resonant tank to cause additional conduction loss. To minimize the circulating current in secondary resonant tank, (12) must be satisfied, which will prohibit the conduction through the undesired path.

$$t_{db\_rise} + t_{delay} \geq \delta_{max} \quad (12)$$

Where, t_{db_rise} denotes the dead-time during turn-on of a secondary MOSFET and t_{delay} is the settling phase delay time, which is the phase difference between primary PWM and secondary PWM in the digital signal processor. Fig. 9 shows the scenario of dead time and phase delay.

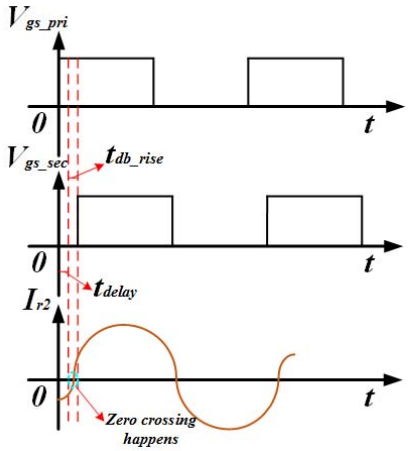


Fig. 9. Theoretical waveforms and phase delay.

Fig. 10 shows the conducting path of circulating current in the secondary side. If the gate pulse of high MOSFET comes earlier than zero crossing of the resonant current, the secondary side resonant current partially circulates through the high-side MOSFET and resonant capacitor (C_{r3}). In addition, a considerable portion of the resonant current takes the path of discharging the battery. This circulation results in additional conduction losses in the secondary MOSFET and transformer winding, which potentially degrades the conversion efficiency. To minimize circulating current in the secondary side, dead band control is introduced so that zero crossing of resonant current occurs within the dead time.

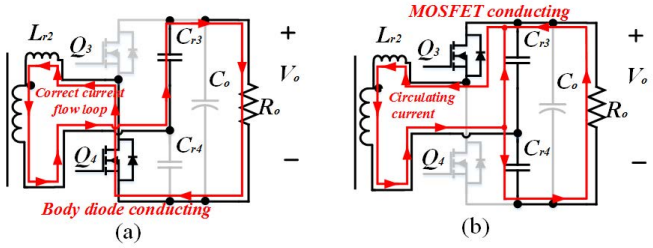


Fig. 10. Circulating current path in the secondary side if (a) gate pulse is appropriately engaged (b) gate pulse is not appropriately engaged.

To implement this methodology, additional margins need to be added to withstand the quantization error, as shown in (13)

$$t_{db\_rise} + t_{on} + t_{db\_fall} + t_{allowance} \geq \frac{1}{2}\frac{1}{f_r} \quad (13)$$

Where, t_{on} and t_{db_fall} denote the turn-on time and dead time during turn-off of the secondary MOSFETs, respectively. $t_{allowance}$ is the additional margin, which is kept at $20ns$.

Moreover, another trade-off should be taken into consideration that the dead time needs to be long enough for handling the worst case within the given frequency range. On the other hand, it is noteworthy to mention that the increase of the dead time degrades the power conversion efficiency and the regulation in CV mode control.

To verify this methodology, a PSIM simulation study and a laboratory experiment with the developed prototype are conducted. Fig. 11 and Fig. 12 show the simulation results and experimental waveforms of dead band control, respectively. Drain-to-source voltage (V_{ds}) during the dead time is higher than that during the conduction period due to the differences in voltage drops between the body diode and MOSFET, as can be seen in Fig. 12.

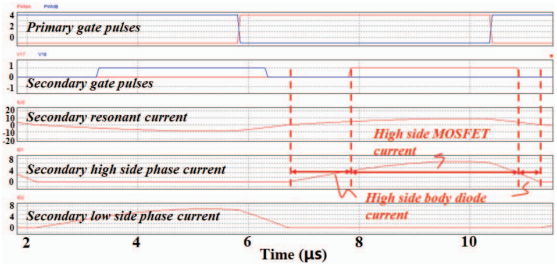


Fig. 11. Simulation results of dead band control.

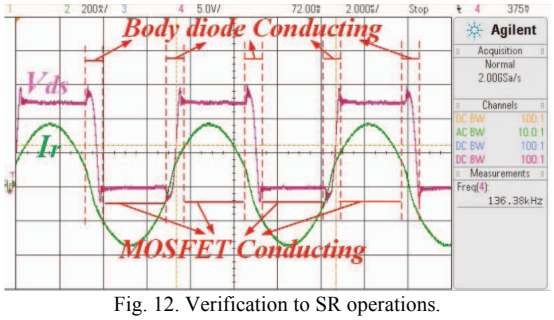


Fig. 12. Verification to SR operations.

V. Experimental Results

As verification to the proof-of-concept, the bidirectional CLLC converter is designed and tested up to $3.3kW$. Photographs of the prototype and the experimental setup are shown in Fig. 13 and Fig. 14, respectively. The power density of the prototype is $1kW/L$ and the gravimetric power density is $0.9kW/kg$.

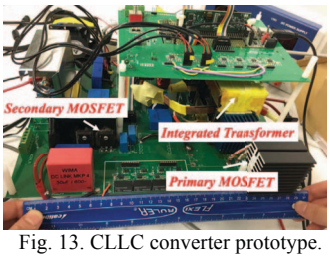


Fig. 13. CLLC converter prototype.

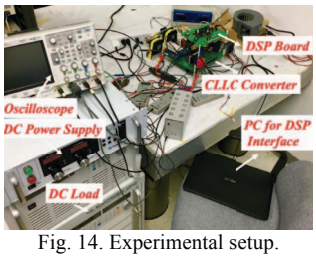


Fig. 14. Experimental setup.

Fig. 15 shows the steady state waveforms of the CLLC converter operating at $3.3kW$ with 110 kHz switching frequency. The output voltage and output current are regulated at 400V and 7.54A, respectively at an input of 600V.

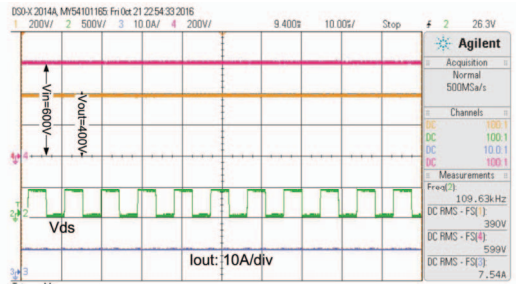
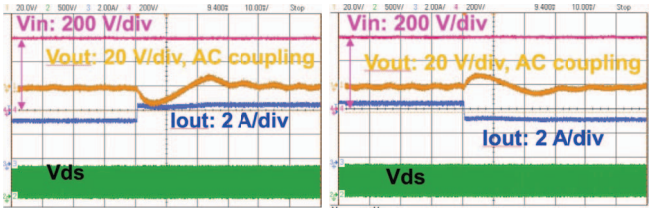


Fig. 15. Experiment result at $3.3kW$ output power in CV mode.

In order to verify the effectiveness of voltage loop and current loop design, both step-up and step-down load transients are conducted in the experiment. Fig. 16 (a) and Fig. 16 (b) show the closed voltage loop transients from $2kW$ to $1.5kW$ and $1.5kW$ to $2kW$, respectively. Output voltage is settled at its reference level i.e. 400V within 30ms for both the cases.



(a) (b)

Fig. 16. Waveforms obtained using CLLC voltage loop control (a) step-down from $2kW$ to $1.5kW$ (b) step-up from $1.5kW$ to $2kW$.

Fig. 17 shows the measured efficiencies of the converter with and without SR at a switching frequency of 150 kHz and input voltage of 600V. As the figure indicates, the efficiency is improved by up to 2% by incorporating the proposed SR implementation technique on the secondary side.

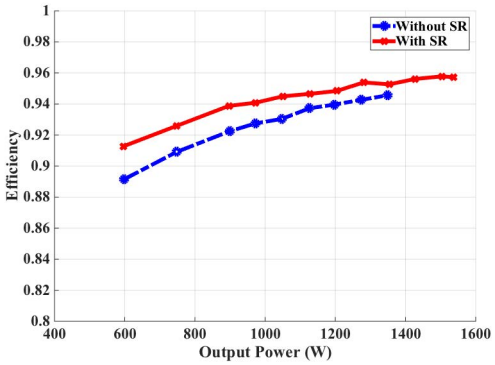


Fig. 17. Efficiency comparison between the CLLC converter with SR and without SR.

Fig. 18 shows the efficiency curves of the CLLC G2V and V2G modes across a wide load range. The peak efficiency of G2V mode is 97.5% at 1.6kW while the peak efficiency of V2G mode is 97.3% at 650W. Table 3 lists the key parameters for the operation in G2V and V2G modes.

Table 3. Key designed parameters for G2V and V2G modes

Parameters	G2V	V2G
Input voltage (V)	600	400
Output voltage (V)	420	600

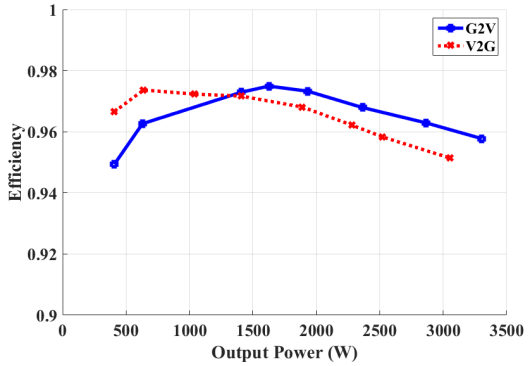


Fig. 18. Efficiency comparison between the CLLC G2V mode and V2G mode.

VI. Conclusions

In this paper, an innovative SR implementation technique in a bi-directional CLLC converter is introduced and analyzed. As a part of the design, resonant parameters are optimized to improve efficiency as well as power density. A closed loop compensation technique utilizing the proposed SR control logic is implemented to realize CV charging and to further improve the conversion efficiency. Experimental results are presented to verify the effectiveness of the control methodology. According to the experimental results, implementation of SR improves the efficiency up to 2%. Thus, the peak efficiencies of G2V and V2G modes reach 97.5% at 1.6kW and 97.3% at 650W, respectively.

VII. Acknowledgement

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