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A Combinational Level Shifted and Phase Shifted PWM Technique for Symmetrical Power Distribution in CHB Inverters

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Abstract— **In Cascaded H-Bridge (CHB) Multilevel inverters (MLI), the application of Phase Shifted Pulse Width Modulation (PSPWM) and Level Shifted Pulse Width Modulation (LSPWM) are the two prominent techniques to attain the multilevel as well as better performance. But both of them have certain drawbacks like in PSPWM the switching loss of all the semiconductors are high and in LSPWM the power-sharing between the cascaded modules is not identical. These two drawbacks have been addressed in this paper by proposing a novel modulation technique, named the Phase Opposed Disposed Phase Shifted PWM (PODPSPWM). In this technique, the level-shifted carriers have been rotated in such a way that there should not be any active power loss and simultaneously the carriers are phase-shifted as per the PSPWM technique. A detailed mathematical analysis of switching loss for all three methods has been presented. Moreover, the power-sharing as well harmonic spectrum of proposed PODPSPWM over other PWMs have been discussed. This novel modulation technique has been simulated in the MATLAB/Simulink software to validate the superiority of the operation. The 1.5kW Experimental prototype is developed and validated the performance of the proposed PODPSPWM modulation.**

Index Terms — Carrier rotation, Cascaded H – Bridge Inverter, Multilevel inverter, Level – Shifted PWM, Phase – Shifted PWM, Power Distribution, Switching loss analysis.

I. Introduction

In renewable as well as electric drives applications, the enhanced prominence on the ability to handle high voltage with reduced switch stress and an improved output voltage profile with minimized filter requirement has enforced towards the multilevel inverters (MLI) [1]-[5]. The other benefits of MLIs are, lower EMI issues, reduced common-mode voltages, etc., The diode clamped (DC), Flying capacitor clamped (FCC) and cascaded H-Bridge (CHB) MLIs are the well-known multilevel inverters, as introduced three decades back [1]. In these MLIs, the high voltage input DC is scale-downed into lesser magnitudes by using passive or semiconductor devices, which helps in the realization of the multilevel voltage at the output side [2]-[5]. Among the all three well-known MLIs, the CHB MLI is finding incredible interest in renewable applications, because of simple in control, sustainability for high voltage handling like few hundreds of kV to MV, higher fault tolerance due to its modularity structure, and free from the capacitor balancing issues [5]-[6]. Moreover, the isolated DC source for each H-bridge module of CHB MLI adds a significant advantage to practical applicability in PV, fuel cell applications.

In the CHB MLI, the individual H-Bridge (HB) module is capable of generating the 3-level output voltage. To generate a higher number of levels in voltage at the output side, multiple HB modules are connected in a cascaded manner [5]-[6]. For CHB MLI, the generic sinusoidal pulse width modulation (PWM) techniques are level shifted PWM (LS PWM) or phase-shifted PWM (PSPWM), i.e., used to get the better quality of output [7]-[11]. In the PSPWM controlled CHB MLIs, a phase shift between the carriers has been provided to get a multi-level as well as an improved harmonic profile of output voltage. Here all HB modules are switched in the entire duration of a fundamental cycle, which results in the equal power distribution among all the HB modules as well as higher switching loss. Because of the displaced/phase-shifted carriers, in PSPWM the switching harmonics have appeared at the multiples of N*switching frequency (where N=number of cascaded H-bridge modules or number of inverter legs/phase) [11]-[12].

The phase disposition (PS), phase opposition disposition (POD), and alternate phase opposition disposition (APOD) are the different possible PWMs in the class of LSPWM, which are categorized depends on the carrier displacement [7]-[9]. With the symmetrical LSPWM modulated CHB MLI, for generating a multilevel voltage, the modules are switched in an unsymmetrical manner. For an instance, in a 7-level CHB inverter, the top module will pump the energy to load during the entire fundamental cycle (i.e., 100% in terms of the time period (TP)), whereas the bottom module will pump the energy for peak voltage levels only (33% of TP) and the middle module will pump the energy for intermediate and high voltage levels (66% of TP) [9]. Because of this, in LSPWM the switching losses are minimal. The unequal switching of HB modules in CHB MLI will result in the uneven power distribution of the DC sources. Moreover, in the LSPWM the switching harmonics have appeared at all multiples of the switching frequency, which may increase the filter size requirements [9],[11]-[12].

In the literature [13]-[28], different LSPWMs, as well as different energy balancing techniques, have been stated for MLIs for achieving equal power distribution or equal voltage balancing. To attain the balancing the capacitor voltages, the carrier rotation strategy is reported for FCC MLIs in [13]-[15]. In these works, LS-PWM is used by incorporating the single carrier rotation and trapezoidal type of carrier rotation along with phase shift has implemented. With the advantage of this carrier rotation strategy, the first foot towards even power distribution in CHB MLIs by using modified PD-LSPWM is presented in [16]. In this modified PD-LSPWM, the carriers associated with HB modules are rotated symmetrically after every switching time period (i.e., after one cycle of a carrier wave). In [17], different types of the carrier rotated PWM are presented for CHB MLIs, i.e., 1) the carrier is rotated in every fundamental sine wave cycle, 2) the carrier is rotated in every

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carrier wave cycle, in these two types PWMs the carrier is rotated symmetrically from top to bottom (from +ve to –ve voltage levels).

Later different LSPWMs (either PD or POD) with carrier rotation strategies are presented for CHB MLIs for even power distribution among HB modules [18]-[25]. For PV fed CHB grid integrated MLIs, a modified carrier rotation strategy is presented for balancing the energy among all PV connected HB modules, where the carrier is rotated in 1:2:3 ratios of uniform time durations, i.e., 1st rotation of carrier after 6 switching/ carrier wave cycles and 2nd rotation is after 12 switching cycles and follows symmetrically [20]. The detailed comparative study of LSPWM and PSPWM, as well as different carrier permutation techniques of LSPWM for balancing the power under different unbalance conditions, is given in [22]. With the help of switching redundancies of the MLI, another type of energy balancing scheme is presented in [26], where the authors are used simple LSPWM. Recently, a modified LSPWM with one, two, and three-cycle rotations (carrier wave cycles) of a carrier in APOD PWM for equalizing the power among the modules of quasi Z-source cascaded MLIs [27]-[28]. Here, detailed comparative analysis with the associated pros and cons for a different number of cycle rotations in LSPWM is presented. However, in the literature [13]-[28], different carrier rotated PWMs presented for even power distribution but the optimal number of cycles to rotate the carriers, switching loss analysis, and associated mathematical support, a suitable type of PWM like PD or POD or APOD are not presented clearly.

To address the above issues, in this paper a carrier rotated as well as phase-shifted PODPSPWM is proposed with equal power distribution for 7-level CHB MLIs. The proposed PODPSPWM is realized with the combination of both LSPWM and PSPWM. Apart from the equal power distribution, the proposed PODPSPWM technique will comprise the minimized magnitude of switching harmonics similar to PSPWM as well as minimized switching loss similar to LSPWM. In this paper the detailed comparative study of different PWMs is presented concerning switching loss analysis and the power distribution with supported mathematical evidence is presented.

II. Proposed PWM Technique

For verification of the proposed pulse with modulation (PWM) technique, three H – Bridge modules are cascaded to obtain seven–level output voltage as shown in Fig. 1. Here, the RL load is connected to the inverter output. To obtain the desired output RMS voltage, the input dc voltage required for each module is given by:

$$V_{dc} = \frac{V_{rms} * \sqrt{2}}{m * N} \quad (1)$$

where V_{dc} is the input dc voltage of each CHB module, V_{rms} is the inverter output RMS voltage, m is the modulation index and N denotes the number of operating modules.

To achieve multilevel output, different modulation techniques can be applied. PSPWM and LSPWM are the most popular techniques employed in the existing literature to obtain seven-level inverter output in cascaded H-Bridge configuration.

A. PSPWM (Phase – Shifted PWM)

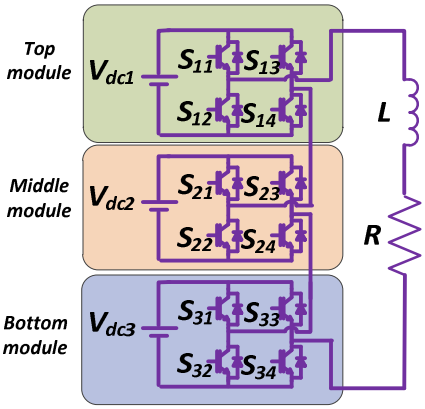

Fig.1. Seven level Cascaded H – Bridge Inverter connected to RL load

In this modulation method, 'N' carrier signals are used for controlling the N number of CHB modules. Here, carrier signals are phase shifted by 180^0/N to achieve multilevel operation. For the seven-level CHB configuration, three signals are phase shifted by 0^0, 60^0, and 120^0 to obtain seven–level output voltage as shown in Fig. 2(a). In each switching cycle, all the operating modules change their output voltage state. This results in most switching losses among all the available modulation methods. Due to this, the output voltage waveform has the most dominant switching frequency harmonic components at $2*N*f_s$ (where f_s is the switching frequency and N is the number of operating H – Bridge modules). In this paper, the switching frequency of the 7-level CHB for all types of PWM techniques is maintained constant i.e., 10kHz (discussed later in the simulation section). Switching pulses for the bottom, middle, and top modules are also shown in Fig. 2(a). Since all the modules are continuously switching throughout the fundamental cycle, all the operating modules contribute equal power to the output.

B. Level – Shifted PWM (LSPWM)

In this modulation method, '2N' carrier signals are employed to control the N number of CHB modules connected in cascade. Here, carrier signals are vertically displaced (uniformly) from each other. In this case, 6 carrier signals are used to generate seven–level output voltage. The magnitude of carrier signals is between 1 to 2/3, 2/3 to 1/3, 1/3 to 0, 0 to -1/3, -1/3 to -2/3, and -2/3 to – 1 as shown in Fig. 2(b). Here, for each switching cycle, only one CHB module switches whereas the other connected modules do not change their output voltage state (i. e., no switching in the other modules). This reflects a decrease in the switching losses, which are lowest compared to any other existing technique (presented in section III). However, switching of modules during particular segments of the fundamental cycle results in unequal power distribution among the operating modules. Here, the bottom module (controlled using carrier signals between ±1/3 to 0) contributes the most power to the output whereas the top module (controlled using carrier signals between 1 to 2/3 and -2/3 to -1) contributes the least significant power and it is also dependent upon the amplitude of modulation index. Switching pulses of different CHB modules for a seven-level CHB system are also shown in Fig. 2(b).

C. Proposed Phase – Opposite Disposed Phase – Shifted

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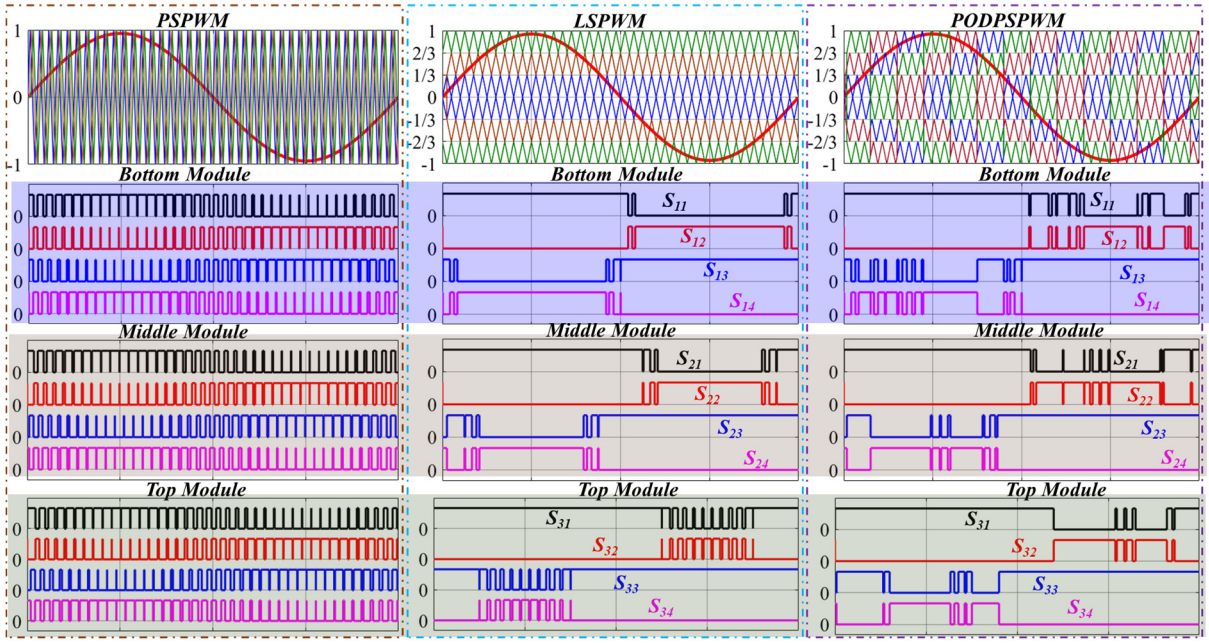

(a) (b) (c)

Fig. 2 – Carrier generation for two modules in (a) PSPWM (b) LSPWM and (c) PODPSPWM with carrier rotation

PWM (PODPSPWM)

As observed, PSPWM results in even power distribution (among operating modules) but high switching losses whereas employing LSPWM leads to minimum switching losses but unequal power distribution between the modules. To harness the benefits of both these modulation methods, the above two modulation methods were mixed, and a new modulation method was proposed. In the proposed PODPSPWM the carrier signals are vertically displaced (similar to LSPWM) as well as phase-shifted by 180^0/N (=60^0 in this case similar to PSPWM) and the carrier rotation technique is also employed for attaining the better performance.

The significant benefits with the proposed PODPSPWM are: (i) Carrier rotation of the carrier signals lead to even power distribution, (ii) Phase shift among the carrier signals will be reflected as improvement in THD content in the harmonic spectrum of the output voltage and load current, (iii) Level shift of the carriers results in minimal switching loss as compared to PSPWM.

Carrier signals for the three modules along with modulation signals are shown in Fig. 2(c). In the proposed PWM, the level-shifted carrier signals are rotated optimally after every three switching cycles. The cycle count is decided based on the switching frequency, discontinuity in the current/power flow at zero crossings, harmonics, switching losses. In this paper, the cycle count is fixed by the trial and error method. In general, if the rotation of carriers is performed after many cycles (>10 or >15), then the current value near zero crossings may become discontinuous owing to a lack of switching or any power flow. This reflects negatively on the harmonic spectrum and filter design. To avoid this, the rotation cycle count must be judiciously selected.

Switching pulses for the bottom, middle, and top modules are shown in Fig. 2(c). Here, in the bottom module, carrier signals are rotated (for every three switching cycles). For demonstration purposes, the low switching frequency of 2 kHz is used. When a high switching frequency is used, the number of cycles in each module will be almost equal which leads to equal power distribution. The contribution of the middle and top modules for three switching cycles can be easily observed in Fig. 2(c). The performance of this modulation method is further exploited in the next section.

III. Switching Loss Analysis

To compare switching losses of switches in different modules when controlled with different modulation methods (PSPWM, LSPWM, and proposed PODPSPWM), the switching table for different switches is presented in Table. I. Here, A indicates the switching action happens for the entire modulation range whereas A/3 indicates the switching action happens only for one–third of the modulation range. Zero indicates that the switch is continuously ON or OFF i.e., no switching in this period. For unipolar switching, each module consists of two types of switches: Type – I and Type – II. Type-I consists of switches S_{11} and S_{13}, which give the same number of switching losses when averaged over a fundamental cycle. Similarly, Type – II consists of switches S_{12} and S_{14}.

For switching loss analysis, each switch type would be selected and its losses are obtained for each module. This switching analysis depends on the period of conduction of the switch when controlled with the defined modulation.

A. *Switching Loss in PSPWM*

In this modulation method, all the switches in all the modules undergo switching for each switching cycle. Due to this, switching losses of all the switches in all the modules (irrespective of Type – I and Type – II) remains the same as shown in Table – I.

Switching loss analysis for switches, when controlled with PSPWM, are given by:

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Table I: Active and shoot – through switching over a fundamental cycle

	PSPWM						LSPWM						PODPSPWM					
	M – 1		M – 2		M – 3		M – 1		M – 2		M – 3		M – 1		M – 2		M – 3	
Modulation Range	S_I	S_{II}	S_I	S_{II}	S_I	S_{II}	S_I	S_{II}	S_I	S_{II}	S_I	S_{II}	S_I	S_{II}	S_I	S_{II}	S_I	S_{II}
0 to $\frac{\pi}{9}$	A	A	A	A	A	A	A	0	0	0	0	0	A/3	0	A/3	0	A/3	0
$\frac{\pi}{9}$ to $\frac{2\pi}{9}$	A	A	A	A	A	A	0	0	A	0	0	0	A/3	0	A/3	0	A/3	0
$\frac{2\pi}{9}$ to $\frac{\pi}{2}$	A	A	A	A	A	A	0	0	0	0	A	0	A/3	0	A/3	0	A/3	0
$\frac{\pi}{2}$ to $\frac{\pi}{2}+\frac{5\pi}{18}$	A	A	A	A	A	A	0	0	0	0	A	0	A/3	0	A/3	0	A/3	0
$\frac{\pi}{2}+\frac{5\pi}{18}$ to $\frac{8\pi}{9}$	A	A	A	A	A	A	0	0	A	0	0	0	A/3	0	A/3	0	A/3	0
$\frac{8\pi}{9}$ to π	A	A	A	A	A	A	A	0	0	0	0	0	A/3	0	A/3	0	A/3	0
π to $\frac{10\pi}{9}$	A	A	A	A	A	A	0	A	0	0	0	0	0	A/3	0	A/3	0	A/3
$\frac{10\pi}{9}$ to $\frac{11\pi}{9}$	A	A	A	A	A	A	0	0	0	A	0	0	0	A/3	0	A/3	0	A/3
$\pi+\frac{2\pi}{9}$ to $\frac{3\pi}{2}$	A	A	A	A	A	A	0	0	0	0	0	A	0	A/3	0	A/3	0	A/3
$\frac{3\pi}{2}$ to $\frac{16\pi}{9}$	A	A	A	A	A	A	0	0	0	0	0	A	0	A/3	0	A/3	0	A/3
$\frac{16\pi}{9}$ to $\frac{17\pi}{9}$	A	A	A	A	A	A	0	0	0	A	0	0	0	A/3	0	A/3	0	A/3
$\frac{17\pi}{9}$ to 2π	A	A	A	A	A	A	0	A	0	0	0	0	0	A/3	0	A/3	0	A/3

$$P = \frac{1}{\pi}\int_0^{\pi} \frac{f_s\,(E_{ON} + E_{OFF} + E_{REC})V_{dc}\,i_{ac}}{V_{ref}\,I_{ref}}\,d\,\omega t \tag{2}$$

where f_s is the switching frequency, E_{ON} and E_{OFF} are the turn-on and turn-off energy losses per pulse of the IGBT, E_{REC} is the reverse recovery loss of the antiparallel diode, V_{ref} and I_{ref} are the switched voltage and current references, V_{dc} is the dc-link peak voltage of each module and i_{ac} is the ac load current [28]. The active switching loss occurring in a CHB multilevel inverter with PSPWM for a fundamental cycle is given,

$$P = \frac{P_{FAC}}{\pi}\int_0^{\pi} \mathrm{I_m}\,\mathrm{Sin}\,\omega t d\,\omega t \tag{3}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\left(-\mathrm{Cos}\,\omega t\right)\Big|_0^{\pi}\right] \tag{4}$$

$$P = \frac{2P_{_{FAC}}\,\mathrm{Im}}{\pi} \tag{5}$$

where the $\mathrm{P_{FAC}} = \frac{f_s(E_{ON}+E_{OFF}+E_{REC})V_{dc}}{V_{ref}\,I_{ref}}$ is the active power loss coefficient, $\mathrm{I_m}$ is the peak value of ac load current. Eq. (5) gives the full load switching losses happening in a fundamental switching cycle. This value is selected as a benchmark value (i.e., 100%) for comparison with other switching methods.

B. Switching Loss in LSPWM

In this modulation method, for a given modulation region, only one module would be switching. Other modules may be completely ON or completely OFF as shown in Table – I. For example, in the modulation range 0 to $\frac{\pi}{9}$, the only Type – I switches of Module I are conducting. Other switches are completely OFF.

For comparison with PSPWM, switching losses are determined for half the fundamental cycle. Active switching losses for devices in Module I is given by the Eq. (3) and the respective equations will be given from Eq. (6) to Eq. (9).

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\int_0^{\pi/9} \mathrm{Sin}\,\omega t d\,\omega t + \int_{8\pi/9}^{\pi} \mathrm{Sin}\,\omega t d\,\omega t\right] \tag{6}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\left(-\mathrm{Cos}\,\omega t\right)\Big|_0^{\pi/9} + \left(-\mathrm{Cos}\,\omega t\right)\Big|_{8\pi/9}^{\pi}\right] \tag{7}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\mathrm{Cos}\,0 + \mathrm{Cos}\left(8\pi/9\right) - \mathrm{Cos}\left(\pi/9\right) - \mathrm{Cos}\left(\pi\right)\right] \tag{8}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[0.1206\right] \tag{9}$$

$P = 6\%$ of switching losses in conventional PWM.

Active switching losses for devices in the module – II are given by Eq. (3) and the respective equations will be given from Eq. (10) to Eq. (13).

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\int_{\pi/9}^{2\pi/9} \mathrm{Sin}\,\omega t d\,\omega t + \int_{\pi/2+5\pi/18}^{8\pi/9} \mathrm{Sin}\,\omega t d\,\omega t\right] \tag{10}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\left(-\mathrm{Cos}\,\omega t\right)\Big|_{\pi/9}^{2\pi/9} + \left(-\mathrm{Cos}\,\omega t\right)\Big|_{\pi/2+5\pi/18}^{8\pi/9}\right] \tag{11}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\mathrm{Cos}\left(\pi/9\right) + \mathrm{Cos}\left(14\pi/18\right) - \mathrm{Cos}\left(2\pi/9\right) - \mathrm{Cos}\left(8\pi/9\right)\right] \tag{12}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[0.3473\right] \tag{13}$$

$P = 17.36\%$ of switching losses in conventional PWM.

Active switching losses for devices in module – III is given by the Eq. (3) and the respective equations will be given from Eq. (14) to Eq. (17).

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\int_{2\pi/9}^{\pi/2} \mathrm{Sin}\,\omega t d\,\omega t + \int_{\pi/2}^{14\pi/18} \mathrm{Sin}\,\omega t d\,\omega t\right] \tag{14}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\left(-\mathrm{Cos}\,\omega t\right)\Big|_{2\pi/9}^{\pi/2} + \left(-\mathrm{Cos}\,\omega t\right)\Big|_{\pi/2}^{14\pi/18}\right] \tag{15}$$

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$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\mathrm{Cos}\left(2\pi/9\right) - \mathrm{Cos}\left(14\pi/18\right)\right] \tag{16}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[1.5321\right] \tag{17}$$

$P = 76.6\%$ of switching losses in conventional PWM.

C. Switching Loss in PODPSPWM:

The number of cycles in each output voltage level in a modulation region is given by:

$$\text{No. of cycles} = \frac{fs}{f_m * 2\pi} * \left[\mathrm{Sin}^{-1}\left(\frac{m+1}{N}\right) - \mathrm{Sin}^{-1}\left(\frac{m}{N}\right)\right] \tag{18}$$

where f_s is the switching frequency; f_m is the modulation frequency; N represents the number of CHB modules; m = 0, 1,2 represents modulation range from 0 to 1/3, 1/3 to 2/3, and 2/3 to 1 respectively.

For switches in this PWM Method, active switching losses in the devices are given by Eq. (3) and the respective equations will be given from Eq. (19) to Eq. (21).

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\begin{array}{l} \int_{0}^{\pi/27} \mathrm{Sin}\,\omega t\,d\omega t + \int_{\pi/9}^{4\pi/27} \mathrm{Sin}\,\omega t\,d\omega t + \\ \int_{2\pi/9}^{17\pi/54} \mathrm{Sin}\,\omega t\,d\omega t + \int_{\pi/2}^{\pi/2+5\pi/54} \mathrm{Sin}\,\omega t\,d\omega t \\ + \int_{\pi/2+5\pi/18}^{\pi/2+17\pi/54} \mathrm{Sin}\,\omega t\,d\omega t + \int_{8\pi/9}^{8\pi/9+\pi/27} \mathrm{Sin}\,\omega t\,d\omega t \end{array}\right] \tag{19}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[\begin{array}{l} \mathrm{Cos}\,0 + \mathrm{Cos}\left(\pi/9\right) + \mathrm{Cos}\left(2\pi/9\right) + \\ \mathrm{Cos}\left(14\pi/18\right) + \mathrm{Cos}\left(8\pi/9\right) - \mathrm{Cos}\left(\pi/27\right) \\ -\mathrm{Cos}\left(4\pi/27\right) - \mathrm{Cos}\left(17\pi/54\right) - \\ \mathrm{Cos}\left(44\pi/54\right) - \mathrm{Cos}\left(25\pi/27\right) \end{array}\right] \tag{20}$$

$$P = \frac{P_{FAC}\,\mathrm{Im}}{\pi}\left[0.659\right] \tag{21}$$

$P = 32.95\%$ of switching losses in conventional PWM.

For comparison, switching losses obtained with different modulation methods are tabulated in Table II.

Table II: Switching loss comparison for different modulation methods

PWM	Module – 1		Module – 2		Module – 3	
	S_I	S_{II}	S_I	S_{II}	S_I	S_{II}
PSPWM	100%	100%	100%	100%	100%	100%
LSPWM	6%	6%	17.4%	17.4%	76.6%	76.6%
PODPS	33%	33%	33%	33%	33%	33%
PWAM	50%	13.4%	50%	13.4%	50%	13.4%

Insights/Characteristics of each PWM algorithm				
PWM	Power Sharing	Switching Losses	Heatsink Cost	THD
PS	Equal	Highest	Simple	Lowest
LS	Unequal	Least	Complex	Lower
PWAM	Equal	Least	Complex	Highest
PODPS	Equal	Least	Optimal	Moderate

From this table, it can be observed that the switching loss occurring in each module has been reduced by 3 times as compared with conventional PSPWM (i.e., 100% to 33%). In the LSPWM, unequal power-sharing results in unequal switching losses, which are overcome in the proposed PODPSPWM. A detailed discussion on the power-sharing of different CHB modules is presented in the results section.

IV. Simulation Results

For validation of the proposed modulation method, seven-level CHB is designed for 220V, 7A. The priority here is to compare the harmonic performance of the proposed system with PSPWM and LSPWM. Component specifications for the system are given in Table III.

Table III: Specification for five – level CHB

Component/Parameter	Specifications
Input DC Voltage [V]	110
Modulation Index [pu]	0.95
Switching Frequency [kHz]	10
Load Impedance	30Ω, 30mH

A. THD Performance with PSPWM

Fig. 3(a) shows the harmonic spectrum of output voltage waveform obtained with PSPWM modulation method. It shows THD content of 20.68% for RMS voltage of 220V (313.5V peak) at the fundamental frequency. When a switching frequency of 10 kHz is applied, the most dominant harmonic component (after fundamental frequency) is obtained at 60 kHz (i.e., $2*N*f_s$). This happens due to cascaded operation and proper phase shift introduced among the carrier signals. A similar harmonic spectrum is observed in load current for 7A (9.98A peak) and minimal THD content of 0.09% is observed as shown in Fig. 3(b).

B. THD Performance with LSPWM

Fig. 3(c) shows the harmonic spectrum of output voltage which is like the THD content as PSPWM for 220V. However, the dominant frequency component of 10kHz (i.e., f_s) is observed as only one module is switching at a time. In load current also, the dominant frequency of 10 kHz is observed as shown in Fig. 3(d).

C. THD Performance with PODPSPWM

With the proposed PWM method, similar THD content of output voltage is observed as shown in Fig. 3(e). Here also, the dominant frequency component of 10kHz (switching frequency) is observed like LSPWM as only one HB module is switching in each switching frequency, unlike PSPWM where every module switch in each switching frequency. Due to the rotation of carriers, the harmonic component at switching frequency is distributed in the immediate neighborhood as observed in the harmonic spectrum. However, the magnitude of harmonics at f_s has reduced as compared with the LSPWM which can be observed from Fig. 3(b) and (c).

Load current harmonic spectrum also shows a frequency component at 10kHz with a THD content of 0.44% for 7A RMS current. Thus, it can be concluded that the proposed PWM method gives similar harmonic content (as that of PSPWM and

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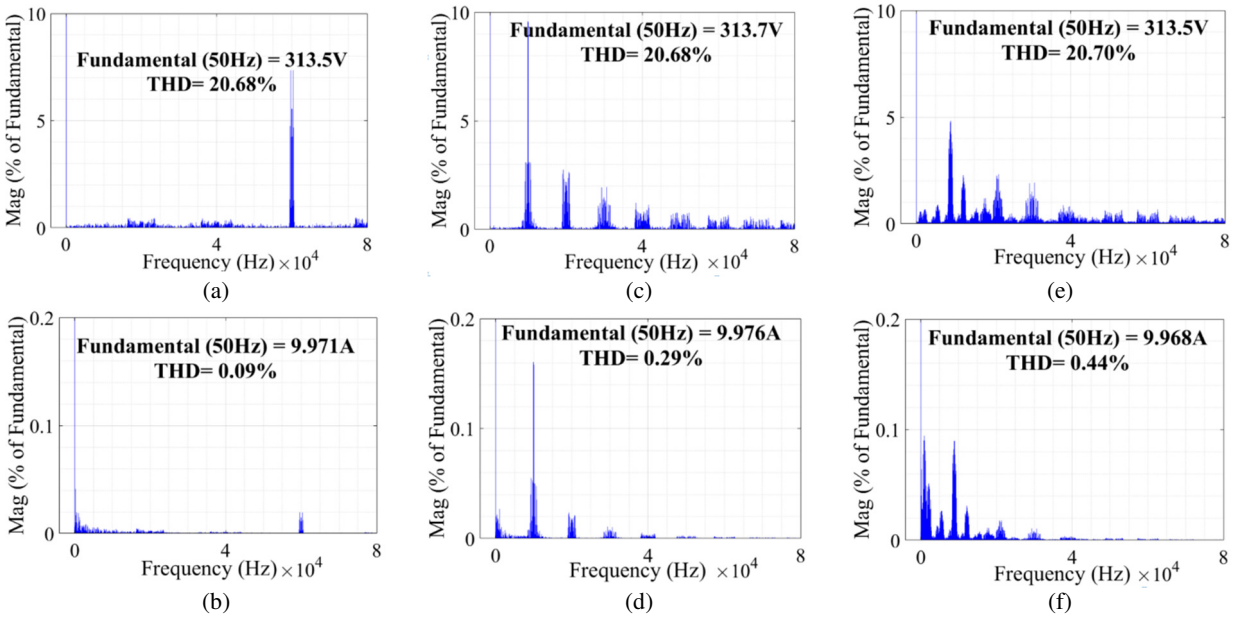

Fig. 3. Harmonic spectrum of output voltage for (a) PSPWM, (b) LSPWM and (c) PODPSPWM (LSPWM with carrier rotation). Harmonic spectrum of load current for (d) PSPWM (e) LSPWM and (f) PODPSPWM.

LSPWM) with lesser switching losses (compared to PSPWM) and even power distribution. For comparison purposes, the values of THD obtained for output voltage and current for different modulation methods are tabulated in Table – IV.

Table IV: Comparison of harmonic spectrum of different modulation methods for output voltage and current

	PSPWM	LSPWM	PODPSPWM
Output Voltage	313.5V (RMS = 221V)	313.7V (RMS = 221V)	313.5V (RMS = 221V)
V_{THD}	20.68%	20.68%	20.70%
Output Current	9.971A (RMS=7A)	9.976A (RMS=7A)	9.968A (RMS=7A)
I_{THD}	0.09%	0.29%	0.44%

D. Verification of Equal Power sharing among operating modules connected in cascade:

Fig. 4(a) shows the input current drawn by the three modules (bottom, middle, and top) along with their respective input current averages and load current for the PSPWM technique. Here, it should be observed that as all the modules switch for each switching cycle, a current waveform obtained in all the modules is the same and the corresponding average current values are also the same. Fig. 4(b) also the module currents and corresponding average values along with load current. With the LSPWM method, the bottom module contributes power for the entire fundamental cycle whereas the middle module remains inactive for the modulation range of 0 to 1/3 and the top module remains inactive during the 0 to 2/3 modulation range. Here, inactive means the voltage contribution of this module during this modulation range is clamped at $+V_{dc}$, and the current value just follows the sinusoidal pattern as observed in the respective subfigures of Fig. 4(b). This unequal switching is also reflected in the average current. Here, the bottom module (carrier signal between 0 and ±1/3) draws the highest current from the power source and its switches are also rated for higher current. Similarly, the current drawn by the middle module is less than the bottom module and the top module draws the least current from the input source.

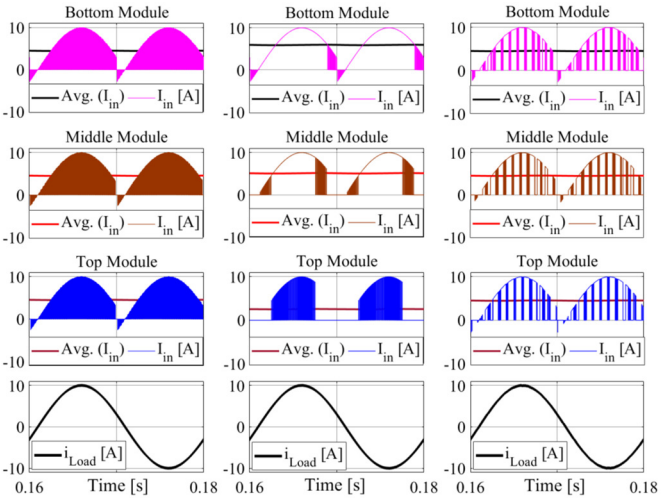

Fig. 4 – Input currents of bottom, middle and top modules along with load current for (a) PSPWM (b) LSPWM and (c) PODPSPWM.

In the proposed PODPSPWM method as shown in Fig. 4(c), rotation is applied on the uniform and vertically displaced carrier signals, and phase-shifted is also applied. This strategy is reflected in the input current drawn by all the operating modules. Initially, just after zero crossings, the input current drawn is continuous in nature. This occurs due to the low current requirement of the modulation signal. However, once the modulation range exceeds 1/3 of modulation amplitude, the input current is obtained as a combination of either direct sinusoidal current or pulse–width modulation sinusoidal current as observed in all input current of all modules. Corresponding average current values indicate equal input current is drawn

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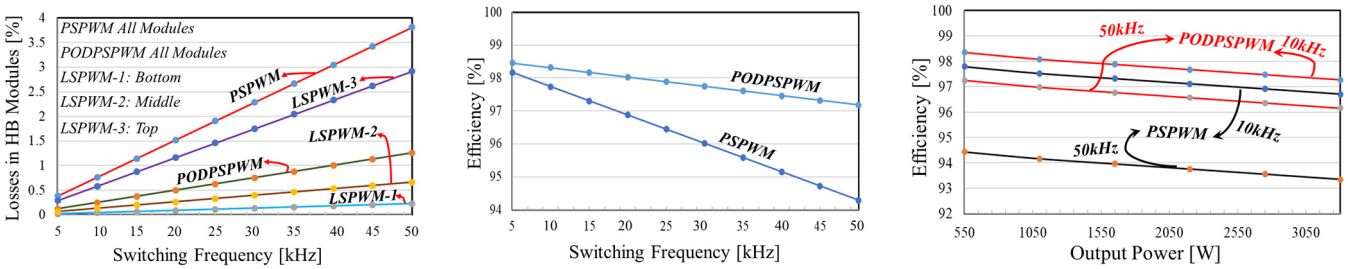

Fig. 5. Variation of (a) % losses and (b) estimated operating efficiency in H-Bridge module for increasing switching frequency with different PWM techniques, and (c) Variation of estimated converter efficiency for variation of output power.

from all the operating modules thereby validating even power distribution with the proposed PWM method.

For performance comparison, switching loss analysis is carried out for different powers and switching frequencies. Fig. 5(a) shows the variation of %losses in modules for increasing switching frequency for different modulation techniques. Here, it can be observed that with PSPWM switching, losses incurred reach nearly 4% for an operating frequency of 50 kHz. The resulting efficiency of the converter modules is shown in Fig. 5(b). It shows an improvement of 3% at an operating frequency of 50 kHz. Fig. 5(c) shows the variation of estimated efficiency for increasing operating power at different frequencies and PWM techniques. It can be observed that using PSPWM at higher frequencies would result in significant power loss (especially at higher output powers).

V. Hardware Results

An experimental prototype for 3.3 kW has been developed in the laboratory to validate the proposed PODPSPWM, as shown in Fig. 6. It is realized with three SiC-based HB modules (connected in cascaded structure), RL–load bank, three DC-power supplies, and Virtex-5 FPGA control board. The experimental prototype testing parameters are Switching frequency: 50 kHz, DC link voltage of each module: 140V DC, 3 SiC modules (CCS050M12CM2), fundamental frequency: 50Hz, 2 series RL loads (25Ω+38mH).

The three-cycle carrier rotation method of PODPSPWM applied to the 7 level CHB, the load voltage and load current waveforms with a step-change in load as well as the type of load are shown in Fig.7, were 280V RMS and the 11.2A RMS current with a 0.95 power factor. The voltage steps of 140V height at every successive level have been achieved which will minimize the THD in the output voltage. The output current is increased by twice when the load is shifted from 2RL (2 series-connected RL loads) to RL load, shown in Fig. 6 (a). The change of load type from R load to RL load results in a change of power factor from unity to 0.95 can be observed in Fig. 6(b). The output voltage, individual module voltages are shown in

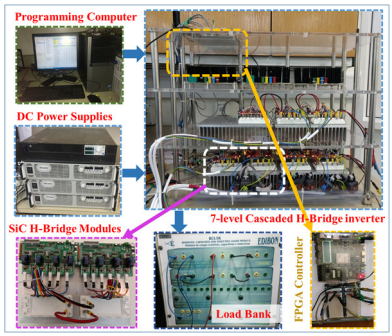

Fig. 6. Experimental prototype of the 7-level CHB inverter

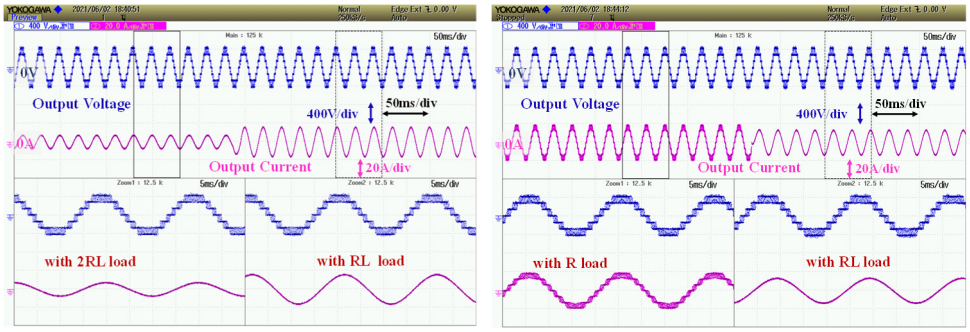

Fig. 7. Seven-level CMI output voltage and output load current waveforms, (a) Load Change from two series RL loads to single RL load, (b) Step change in type of load from R load to RL load step change.

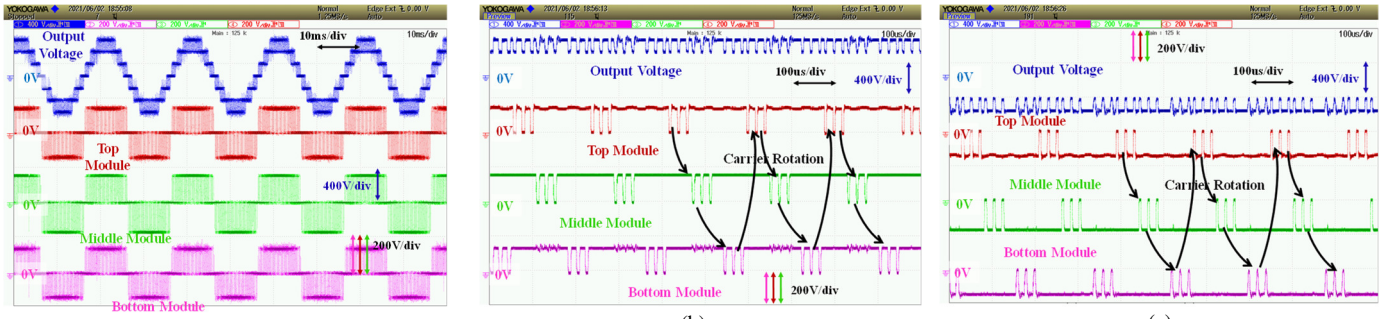

Fig. 8. (a) The bottom, middle and top modules three level output voltages along with their cascaded seven level output voltage, (b) Zoomed positive quarter cycle of Fig. 7(a) shows the carrier rotation of the proposed scheme , (c) Zoomed negative quarter cycle of Fig. 7(a) shows the carrier rotation of the proposed scheme.

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Fig. 8(a), where the peak of each module voltage is 140V and the overall output voltage is 3*140V. As we discussed in the switching types I, II, and III; in Fig. 8(b) the type I and type II can be observed as they are overlapping at the level change of the output voltage. The average switching of all the modules is identical, i.e., the power-sharing between them is also equal.

In Fig. 8(b), the positive cycle is zoomed-in which the proposed carrier rotation is observed. The bottom module harvests the first three output pulses of least width then the conduction is moved to the middle module which then produces the three pulses with slightly increased width. At last, the conduction is shifted to the top module, which produces pulses of further larger width. Again the conduction shifted to the bottom module. This typical carrier rotation occurs up to the modulation reaches the peak of a first carrier signal. While the output voltage is fluctuating between 140V and 280V, the conduction of the modules shifts after the sixth output pulse (due to two modules switching simultaneously). This is known as the Type II modulation region. While the output voltage is fluctuating between 280V and 420V, the conduction of a module never shifts. This is known as the type III modulation region. All three modules are switching for creating a 420V level of the output voltage. It can be observed that all three modules are generating 0V and 140V, but the carriers are phase-shifted by the 120^0 so there is no loss of active voltage levels. Similar rotation happens for the negative half cycle as shown in Fig. 8(c).

In Fig. 8, the output, as well as input voltage and currents, are presented with a step-change in the load from 2RL to RL load. The input current and output current magnitudes are varied according to the load applied on the inverter. The equal power-sharing between the modules has been presented in Fig. 9 and 10, where the experiment is done for various power levels, and showing all the three modules the input currents are approximately equal in nature with respect to the load current.

Fig.10 shows the seven-level output load voltage, individual module output voltage, input voltage, and the individual module input current. Fig. 10(a) shows the top module output voltage of three levels of 140V, 0V, and -140V. The average input current is 8.5A for an applied input voltage of 140V from the DC power supply. It is observed that the input current is in pulsed manned and has a double line frequency component. Middle module output voltage levels are 140V, 0V, and -140V for an applied input voltage of 140V. Input average current of 8.4A is drawn from the power supply as shown in Fig. 9(b). Fig. 9(c) shows the bottom module output voltage of three levels of 140V, 0V, and -140V for an input voltage of 140V. The average input current of 8.6A is drawn from the DC-power supply. Even though the level-shifted modulation is applied, the conduction of the top module is not discontinuous because of carrier rotation.

For demonstration of the experimental efficiency, variation of efficiency for different operating powers (for PWM and PODPSPWM) is shown in Fig. 11. It can be observed that an improvement of at least >2% is observed at all the operating points with peak efficiency of 96% obtained at the rated power.

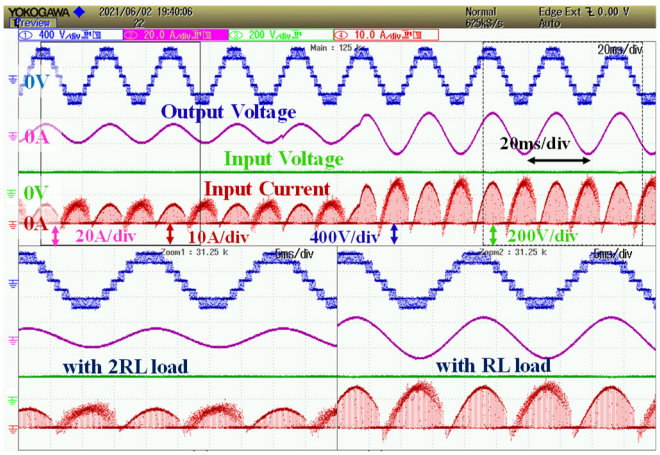


Fig. 9. Input as well as output voltage and current waveforms with step change in load.

VI. Conclusion

A novel PODPSPWM technique for the CHB MLI has been presented in this article. The proposed modulation technique

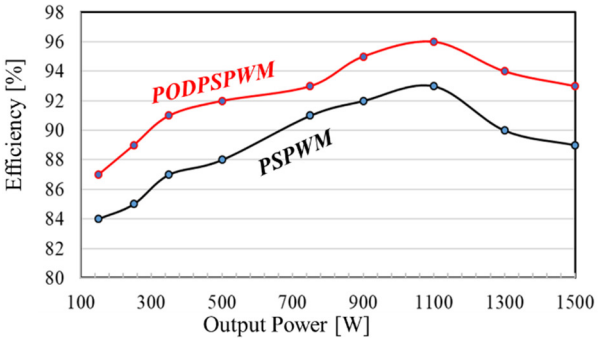
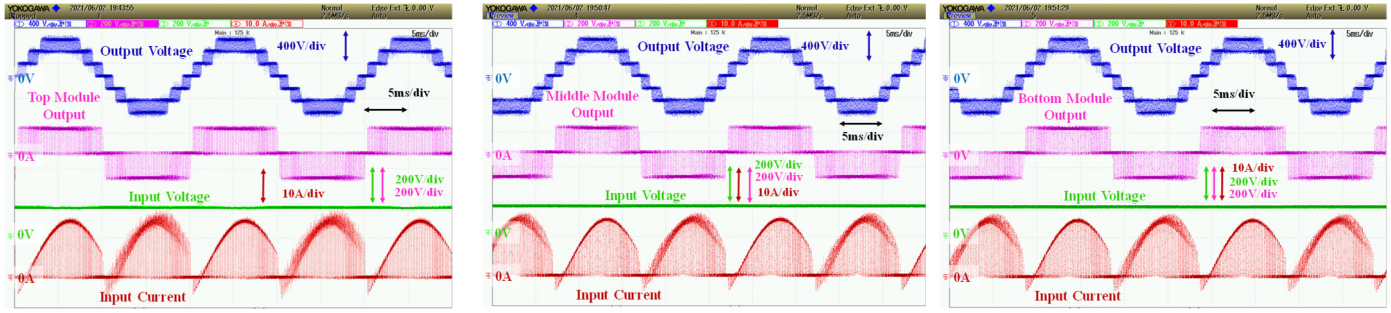


Fig. 11. Variation of experimental efficiency of the developed converter module for different operating output powers



(a) (b) (c)

Fig. 10. Equal power sharing between the modules during the different load currents.

implementation, operation, and comparative analysis with the standard PSPWM and LSPWM techniques are presented. The detailed mathematical switching loss analysis for all the 3 modulation methods is evident that the switching loss is equal in all the semiconductor modules and lesser than the PSPWM. It is also deduced that the reduction of 67% of the switching losses in the proposed PODPSPWM over the PSPWM. Moreover, in the proposed PWM the magnitude of switching frequency harmonics is minimal over LSPWM. The carrier rotation implementation has balanced the power between the modules. The experimental, as well as simulation results, are evidence that the successful implementation and execution of the proposed PODPSPWM. Furthermore, the phase shift between the modules has been incorporated into the modulation to reduce the THD and it also achieves the same THD as that of the standard PWM techniques. The proposed algorithm can be more suitable for solar PV applications to address the shading and uneven power generation between the solar panel modules.

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REFERENCES

[1]. J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," in *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[2]. Franquelo. L.G, Rodriguez. J, Leon. J.I, Kouro. S, Portillo. R, Prats. M.A.M, "The age of multilevel converters arrives", *IEEE Ind. Electron. Magazine*, Volume 2, Issue 2, June 2008, Pages: 28-39.

[3]. S. Kouro et al., "Recent Advances and Industrial Applications of Multilevel Converters," in *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[4]. B. P. Reddy and S. Keerthipati, "A Multilevel Inverter Configuration for an Open-End-Winding Pole-Phase-Modulated-Multiphase Induction Motor Drive Using Dual Inverter Principle," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3035-3044, April 2018.

[5]. Malinowski, K. Gopakumar, J. Rodriguez and M. A. Perez, "A Survey on Cascaded Multilevel Inverters," in *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197-2206, July 2010.

[6]. M. Vijeh, M. Rezanejad, E. Samadaei and K. Bertilsson, "A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View," in *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9479-9502, Oct. 2019.

[7]. B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 858-867, Aug. 2002.

[8]. Y. Li, Y. Wang and B. Q. Li, "Generalized Theory of Phase-Shifted Carrier PWM for Cascaded H-Bridge Converters and Modular Multilevel Converters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 589-605, June 2016.

[9]. R. Naderi and A. Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters," in *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1257-1269, May 2008.

[10]. S. Lu, L. Yuan, K. Li and Z. Zhao, "An Improved Phase-Shifted Carrier Modulation Scheme for a Hybrid Modular Multilevel Converter," in *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 81-97, Jan. 2017.

[11]. D. G. Holmes and B. P. McGrath, "Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverter," in *IEEE Trans. Ind. Appl.,* vol. 37, no. 2, pp. 574-582, Mar/Apr 2001.

[12]. B. P. Reddy and S. Keerthipati, "Linear Modulation Range and Torque Ripple Profile Improvement of PPMIM Drives," in *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 12120-12127, Dec. 2019.

[13]. D. -. Kang, W. -. Lee and D. -. Hyun, "Carrier-rotation strategy for voltage balancing in flying capacitor multilevel inverter," in *IEE Proceedings - Electric Power Applications*, vol. 151, no. 2, pp. 239-248, 9 March 2004.

[14]. Dae-Wook Kang, Byoung-Kuk Lee, Jae-Hyun Jeon, Tae-Jin Kim and Dong-Seok Hyun, "A symmetric carrier technique of CRPWM for voltage balance method of flying-capacitor multilevel inverter," in *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 879-888, June 2005.

[15]. B. P. McGrath, T. Meynard, G. Gateau and D. G. Holmes, "Optimal Modulation of Flying Capacitor and Stacked Multicell Converters Using a State Machine Decoder," in *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 508-516, March 2007

[16]. M. Angulo, P. Lezana, S. Kouro, J. Rodriguez and B. Wu, "Level-shifted PWM for Cascaded Multilevel Inverters with Even Power Distribution," *2007 IEEE Power Electronics Specialists Conference*, Orlando, FL, 2007, pp. 2373-2378.

[17]. D. Sreenivasarao, P. Agarwal and B. Das, "Performance evaluation of carrier rotation strategy in level-shifted pulse-width modulation technique," in *IET Power Electronics*, vol. 7, no. 3, pp. 667-680, March 2014.

[18]. I. Sarkar and B. G. Fernandes, "Modified hybrid multi-carrier PWM technique for cascaded H-Bridge multilevel inverter," *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Dallas, TX, 2014, pp. 4318-4324.

[19]. K. K. Gupta, P. Bhatnagar, H. Vahedi and K. Al-Haddad, "Carrier based PWM for even power distribution in cascaded H-bridge multilevel inverters within single power cycle," *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 6470-6475.

[20]. J. Chavarria, D. Biel, F. Guinjoan, C. Meza and J. J. Negroni, "Energy-Balance Control of PV Cascaded Multilevel Grid-Connected Inverters Under Level-Shifted and Phase-Shifted PWMs," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 1, pp. 98-111, Jan. 2013.

[21]. J. Mei, B. Xiao, K. Shen, L. M. Tolbert and J. Y. Zheng, "Modular Multilevel Inverter with New Modulation Method and Its Application to Photovoltaic Grid-Connected Generator," in *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5063-5073, Nov. 2013.

[22]. P. Sochor and H. Akagi, "Theoretical and Experimental Comparison Between Phase-Shifted PWM and Level-Shifted PWM in a Modular Multilevel SDBC Inverter for Utility-Scale Photovoltaic Applications," in *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4695-4707, Sept.-Oct. 2017.

[23]. F. Sasongko and H. Akagi, "Low-Switching-Frequency Operation of a Modular Multilevel DSCC Converter With Phase-Shifted Rotating-Carrier PWM," in *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5058-5069, July 2017.

[24]. F. Sasongko, K. Sekiguchi, K. Oguma, M. Hagiwara and H. Akagi, "Theory and Experiment on an Optimal Carrier Frequency of a Modular Multilevel Cascade Converter With Phase-Shifted PWM," in *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3456-3471, May 2016.

[25]. S. Sedghi, A. Dastfan and A. Ahmadyfard, "A new multilevel carrier based pulse width modulation method for modular multilevel inverter," *8th International Conference on Power Electronics - ECCE Asia*, Jeju, 2011, pp. 1432-1439.

[26]. M. R. A and K. Sivakumar, "A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7569-7577, Dec. 2015.

[27]. M. Meraj, S. Rahman, A. Iqbal and L. Ben-Brahim, "Common Mode Voltage Reduction in a Single-Phase Quasi Z-Source Inverter for Transformerless Grid-Connected Solar PV Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 1352-1363, June 2019.

[28]. M. Meraj, S. Rahman, A. Iqbal and N. A. Emadi, "Novel Level Shifted PWM Technique for Unequal and Equal Power Sharing in Quasi Z Source Cascaded Multilevel Inverter for PV Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*. doi: 10.1109/JESTPE.2019.2952206.

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