A Novel High Step-Up SEPIC-Based Non-Isolated Three-Port DC-DC Converter Proper for Renewable Energy Applications

Seyyed Mojtaba Taheri, Alfred Baghramian, Seyed Amir Pourseyedi

1

***Abstract*—This summary introduces a new non-isolated high voltage gain SEPIC-based multi-port DC-DC converter. The boosting structures, including voltage lift cell(VLC) and coupled inductor(CI), are employed to increase the voltage gain of the suggested converter, and also the input current of the proposed structure is continuous and has a low ripple, which is appropriate for renewable energy sources. Both inputs of this converter can operate individually or simultaneously. This topology has three ports: the renewable energy source port, the battery port, which is a bidirectional port, and the output port. In this topology, the voltage stress of three MOSFET switches is low. Low voltage stress of switches causes a reduction in their losses and improves the efficiency of this converter. Compared to converters with similar functionality, the minimum number of active switches is used in this structure, which causes reducing the implementation cost and the control structure's complexity. Operating modes of the new topology are explained in this paper. Ultimately, a 100-Watt prototype of the introduced converter is accomplished to validate the clams.**

***Index Terms*—Multi-port converter, High voltage gain, Renewable energy sources.**

I. Introduction

CONVENTIONAL energy sources like fossil fuels are running out, and the importance of renewable energy sources such as solar energy is increasing [1] and have attracted much attention in recent years. In addition, global energy consumption is growing yearly, which causes more fossil fuels to be burned, significantly impacting air pollution, climate change, global warming, and human health. Renewable energy sources have no costs but the initial cost of implementation and do not cause pollution [2]–[4]. However, these resources have several disadvantages, explained in the following. Due to the unstable nature of these resources, it is necessary to use another source as a backup unit, which leads us to multi-input converters. Also, because the voltage level of renewable energy sources such as solar panels and fuel cells is low, a high step-up topology is needed for these sources. Compared to single-input converters, lower cost, better performance, and fewer elements are the advantages of multi-input converters. Multi-port converters are extensively utilized in microgrids, electric hybrid vehicles, and hybrid energy systems [5]–[7].

Seyyed Mojtaba Taheri, Alfred Baghramian, and Seyed Amir Pourseyedi are with the Electrical Engineering(EE) Department, University of Guilan, Rasht, Iran (e-mail: smojtaba_taheri@msc.guilan.ac.ir, alfred@guilan.ac.ir, amirpourseyedi@msc.guilan.ac.ir and the corresponding author for telephone inquiries: +98 912 4860924; fax: +98 13 6690271; e-mail: alfred@guilan.ac.ir).

There are two general categories of multi-input converters, isolated and non-isolated. Multi-winding transformer [8] or CI [9] are used to design isolated converters. Compared to non-isolated converters, isolated converters are designed for high-power applications. Raising the transformer's turn ratio boosts the voltage gain of the converter. Notwithstanding, multi-winding transformers with a high turn ratio have a challenging design process and a high input current. Also, many isolated converters use active bridge structures that increase the number of switches and the cost of implementation [10], [11]. In [12], several isolated multi-input converters are studied.

Non-isolated multi-input converters have a smaller structure, fewer elements, and lower manufacturing costs. In these converters, there is a direct connection between inputs and output. [40] Following are some techniques for designing a non-isolated multi-input converter. One low-cost and straightforward method of designing a non-isolated multi-input converter is to connect different energy sources by a switch to the input terminal of a conventional converter [13]. One of the disadvantages of this method is the impossibility of using resources simultaneously. In [14] and [15] due to the unequal voltage of the power supplies, the first source is connected to the multi-input structure with a diode and other sources with active switches, and these input sources operate separately. Another technique for designing non-isolated multi-input converters is combining different converters [16]. A SEPIC converter is combined with a buck converter in [17] that one of the input sources is bidirectional and can be charged or discharged. In [18] a double-input central capacitor high gain dc-dc converter for renewable energy sources is introduced. In this structure, two buck-boost converters are integrated. Also, their output is connected to the main capacitor, which is in series with two input sources of the converter and provides the output demand. In structures [19] and [20], base structures(buck and boost structure) are used for two unidirectional inputs, and a bridge structure is exerted for energy storage source input. Another typical method is to use voltage or current pulse source cells in series or parallel on a single-input converter. Voltage pulse energy sources are used in series in [21] and [22], and both sources of these converters can operate independently. In [23], two current pulse sources are connected in series; also, this converter is soft-switched. Several multi-port topologies that use current pulse sources in series or parallel in their inputs are analyzed in [24]. Some non-isolated multi-input converters are manufactured by attaching traditional converters' series, parallel, or series-parallel. Many elements are used in this

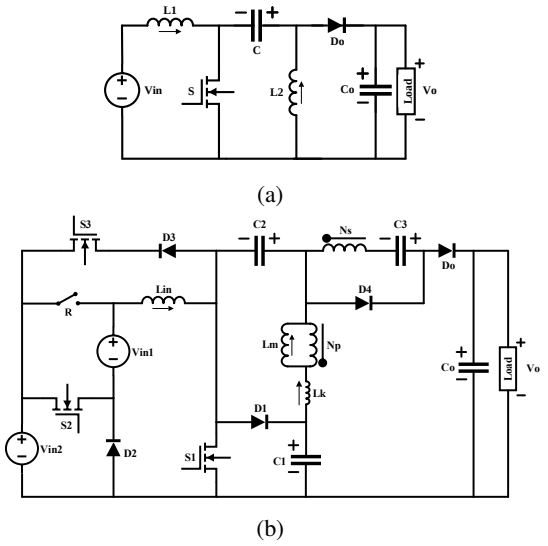


Fig. 1: Presented converter structure. (a) The SEPIC converter. (b) The suggested SEPIC-based non-isolated high step-up multi-port DC-DC converter.

sort of multi-input converter that enhances conduction losses, and as a result, their manufacturing cost increases. Also, the structure becomes complicated. In [25] two buck-boost converters are joined in parallel, and input sources can supply the required output power independently or simultaneously. In structure, [26] two similar converters are connected in series. The operation of this converter is that one of the converters charges a capacitor and the second converter is in series with the charged capacitor, providing output power.

As mentioned, the proposed converter should have a high voltage gain due to the unstable nature and low voltage of renewable energy sources, such as solar panels. The voltage boosting cells, coupled inductor, transformer, etc., are the methods to enhance the voltage gain [27]–[29]. A high gain multi-input dc-dc converter is presented in [30] that input current is discontinuous and two coupled inductors are used to improve the voltage gain, and the power flow of this converter is bidirectional. In [31] a multi-input dc-dc converter is proposed that a switched-capacitor structure is applied in this converter for boosting the output voltage. At the input of this converter, the buck structure is used, and as a result, the input current is discontinuous. A three-port high step-up dc-dc converter is presented in [32]. The energy storage input is bidirectional in this converter. A coupled inductor is used in this structure to increase the voltage gain, but the input current ripple is high.

This article recommends a non-isolated SEPIC-based dual input high voltage gain DC-DC converter, which is illustrated in Fig. 1b. Two voltage boosting structures, a CI and a VLC, are utilized to boost the voltage gain in this converter. The energy storage input of the suggested structure is bidirectional so that it can be charged or discharged, depending on the circumstances. Two inputs of this converter can operate independently or simultaneously. This structure has three active switches. The power switch S_1 faces low voltage stress due

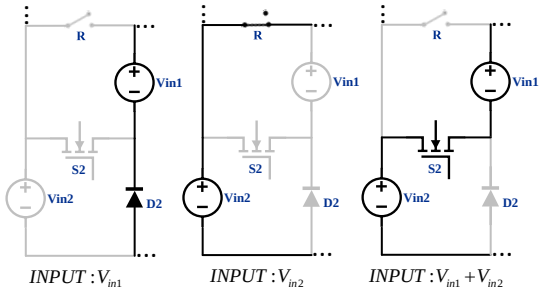


Fig. 2: current flow paths of the input sources of suggested structure in different modes.

to the clamp circuit, and also, Switches S_2 and S_3, by the voltage stress calculations of the semiconductors, withstand low voltage stress. Thus, switches with lower Resistance can be used for the introduced structure, which reduces conduction losses. Compared to the performance of the proposed converter, the minimum number of active switches is used, which reduces switching losses. The current of the first input in all operating modes and the second input in SISO mode is continuous, which is advantageous for renewable energy sources, especially photovoltaic sources. This paper is split into eight sections. The introduction is given in the 1'st section. The offered converter's structure and its modes' explanation are presented in Section II. Section III provides analysis and equations for the structure. Then, the comparison of the suggested topology with similar structures is listed in section IV. The experimental results of the proposed structure are shown in Section V. Ultimately, in Section VI, the conclusion is explained.

II. OPERATION MODES OF THE INTRODUCED STRUCTURE

The SEPIC converter and the presented structure are illustrated in Fig. 1. The seggested topology is based on the SEPIC converter and includes two inputs, three switches, five diodes, four capacitors, an inductor, and a CI. The bidirectional input of this converter is proper for energy storage sources. The other input is continuous current in all modes and is appropriate for photovoltaic sources. According to the calculations, the suggested topology's stress voltage of three MOSFET switches is low. Hence, the losses of these elements are reduced. A CI and a VLC are utilized to boost the output voltage gain in the presented structure. Another merit of this topology is the ability to operate each one of the converter inputs independently or synchronously. Fig. 2 displays how input sources connect in different modes. Several assumptions are made to simplify converter analysis:

1. Capacitors are large enough to ignore voltage ripples.
2. The current ripple of the inductors is ignored.
3. All semiconductors, including switches and diodes, are ideal.

In all modes, the secondary side current of the CI, the CI turn ratio, and the coefficient of coupling are calculated according to the following equation:

$$I_{LS} = \frac{I_{Lm} - I_{Lk}}{N} \tag{1}$$

$$N = \frac{N_S}{N_P} \tag{2}$$

$$k = \frac{L_m}{L_m + L_k} \tag{3}$$

A. SISO and DISO modes

In SISO mode, just one of the sources, first input source V_{in1} through the diode D_2 or second input source V_{in2} through the relay R, transmits energy to the output. When relay R is on, for source V_{in2} to operate appropriately in SISO mode and diode D_2 to remain off, the voltage of source V_{in2} must be higher than the voltage of source V_{in1}. In DISO mode, both inputs operate simultaneously, and the second input plays a supporting role when the first input does not have sufficient power to supply the output demand. Due to the similar function of the SISO and DISO modes, both are discussed in this section. The equivalent circuits and waveforms of intervals are illustrated in Fig. 3a and Fig. 3b, sequentially.

Interval 1 (t_1-t_2): In this short period, switches S_1 and S_2 are turned on. Both inputs are involved in charging the input inductor. Thus, the input inductor current raises linearly. The CI secondary side current feeds the output capacitor and the load through the diode D_o. Due to the high voltage on the small value of the leakage inductor (LI), its current increases with a high slope. The stored energy of the LI is transmitted to the capacitor C_1. The equations of this interval are written below:

$$I_{S1} = I_{Lin} - I_{Lk} - I_{Ns} \tag{4}$$

$$V_{Lm} = k(V_{C1} - V_{C2}) \tag{5}$$

$$V_{Lin} = V_{in1} + V_{in2} \tag{6}$$

Interval 2 (t_2-t_3): At $t = t_2$, the current of the LI transcends the current of the MI. Hence, the diode D_4 is turned on. The stored energy of the capacitor C_1 charges capacitor C_2 and raises the LI current and the MI current linearly. Both input sources charge the input inductor, and capacitor C_o feeds the load. The equations for this section are as follows:

$$V_{Lm} = k(V_{C1} - V_{C2}) \tag{7}$$

$$V_{Lin} = V_{in1} + V_{in2} \tag{8}$$

$$I_{D4} = I_{Ns} = \frac{I_{Lk} - I_{Lm}}{N} \tag{9}$$

Interval 3 (t_3-t_4): In this period, the switch S_2 is turned off, and the diode D_2 is turned on. Therefore, only source V_{in1} charges the input inductor. The rest elements of the presented converter operate as the previous interval. At last, the switch S_1 is turned off. The equations of this interval are written below:

$$V_{Lm} = k(V_{C1} - V_{C2}) \tag{10}$$

$$V_{Lin} = V_{in1} \tag{11}$$

Interval 4 (t_4-t_5): At $t = t_4$, the switch S_1 is turned off and diodes D_2 and D_4 are in direct bias. The inductor L_{in} is discharged in the capacitor C_1 through the diode D_1 . Also, the voltage stress of switch S_1 is significantly decreased by the clamp structure consisting of capacitor C_1 and diode D_1.

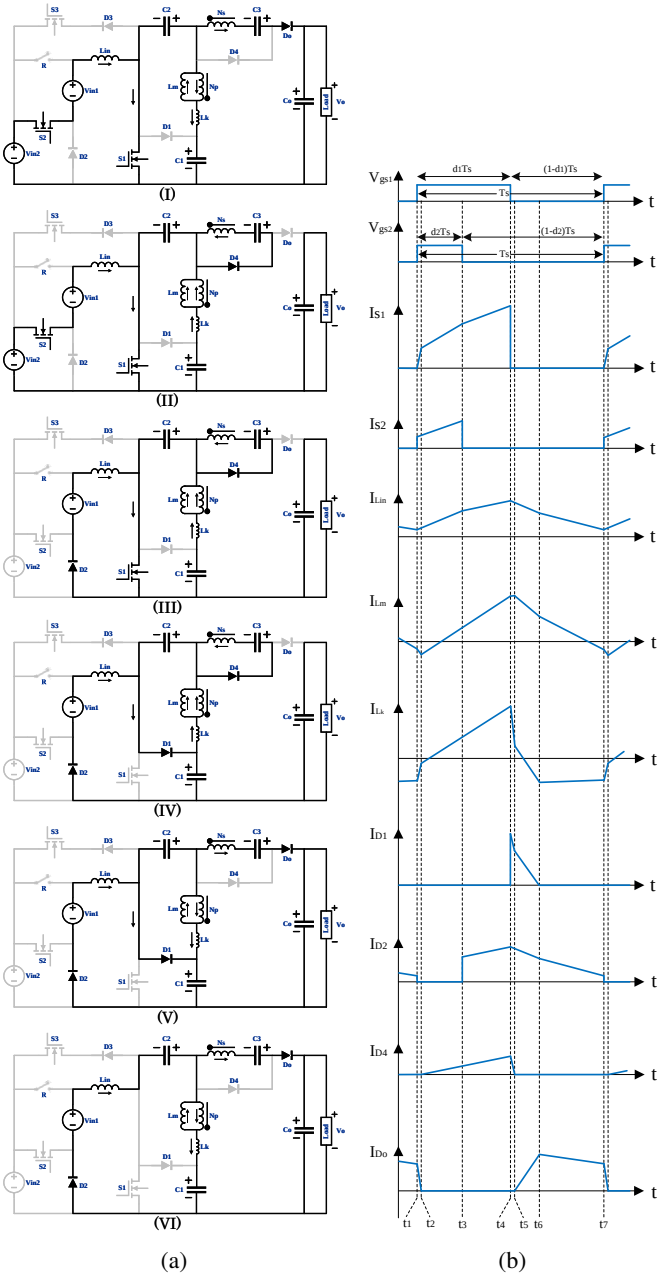


Fig. 3: (a) Equivalent circuit of each interval in DISO mode, (I) interval 1, (II) interval 2, (III) interval 3, (IV) interval 4, (V) interval 5, (VI) interval 6, (b) Steady-state waveforms of the presented structure in DISO mode.

Also, LI energy is recovered via capacitor C_2 through the diode D_1. As described in interval 1, a large negative voltage on the LI causes a large current with a negative slope during this period. The capacitor C_o supplies the output load demand. The equations of this period are as below:

$$V_{Lm} = -kV_{C2} \tag{12}$$

$$V_{Lin} = V_{in1} - V_{C1} \tag{13}$$

Interval 5 (t_5-t_6): In this interval, inductors L_k, L_m and L_{in} are being discharged. At instant t_5, the current of the LI becomes smaller than the current of the MI. Hence, diode

D_4 is turned off, and diode D_o is turned on. Energies of the input source V_{in1}, the input inductor L_{in}, capacitors C_2 and C_3 and the CI secondary side are transmitted to the capacitor C_o and the load via the diode D_o. At the end of this interval, the sum of the currents I_{Lk} and I_{Ns} overtakes the current I_{Lin}. As a result, the current of diode D_1 becomes negative, and this diode turns off naturally. The following equations are represented in this period:

$$V_o = V_{C1} + V_{C2} - V_{Ns} + V_{C3} \tag{14}$$
$$V_{Lm} = -kV_{C2} \tag{15}$$
$$V_{Lin} = V_{in1} - V_{C1} \tag{16}$$
$$I_{D1} = I_{Lin} - I_{Lk} - I_{Ns} \tag{17}$$

Interval 6 (t_6-t_7): At the last interval, the output diode D_o is still on. The energy is transmitted from the input to the output like in the previous interval. This period ends when the switch S_1 turns on. The equations of this interval are written below:

$$V_o = V_{in1} - V_{Lin} + V_{C2} - V_{Ns} + V_{C3} \tag{18}$$
$$V_{Lm} = k\frac{V_{C1} + kN(V_{C1} - V_{C2}) - V_o}{1 + kN} \tag{19}$$

B. SIDO mode

In this mode, the output energy requirement is less than the energy received from photovoltaic source V_{in1}, so the excess energy of this source is stored in energy storage source V_{in2} through diode D_3, and switch S_3. In all periods of this mode, the switch S_2 is off, and diode D_2 is on. The presented topology in SIDO mode has six intervals. The equivalent circuits of this mode are indicated in Fig. 4a, and the waveforms of this mode are represented in Fig. 4b.

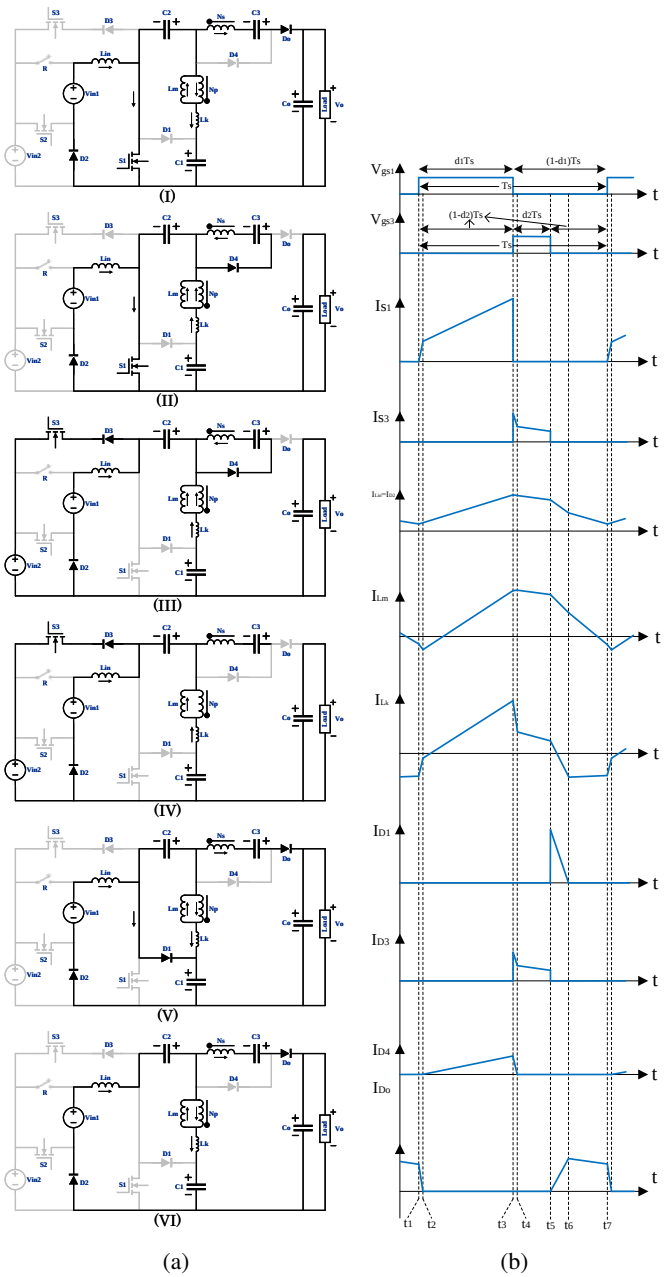
Interval 1 (t_1-t_2): In this short period, the switch S_1 is turned on. Also, diodes D_2 and D_o are in direct bias. The inductor L_{in} is charged by the source V_{in1}, and its current increases linearly while the MI current decreases. The L_{Lk} inductance value is small, and the voltage across it is high; therefore, its current increases with a high slope. The equations of this interval are as follows:

$$V_{Lm} = k(V_{C1} - V_{C2}) \tag{20}$$
$$V_{Lin} = V_{in1} \tag{21}$$
$$I_{S1} = I_{Lin} - I_{Ns} - I_{Lk} \tag{22}$$

Interval 2 (t_2-t_3): At the start of this interval, the LI current exceeds the MI current. As a result, diode D_o is turned off, and D_4 is turned on. Therefore, the capacitor C_3 is energized by the secondary side of CL. The input inductor current increases linearly; also, the energy of the capacitor C_1 is transmitted to the capacitor C_2. The output capacitor C_o feeds the load. The equations of this interval can be obtained as follow:

$$V_{Lm} = k(V_{C1} - V_{C2}) \tag{23}$$
$$V_{Lin} = V_{in1} \tag{24}$$
$$I_{D4} = I_{Ns} = \frac{I_{Lk} - I_{Lm}}{N} \tag{25}$$

Interval 3 (t_3-t_4): This short period begins when switch S_1 is turned off. Also, switch S_3 is turned on, and the stored energy of the input inductor charges the storage source V_{in2} through



(a) (b)

Fig. 4: (a) Equivalent circuit of each interval in SIDO mode, (I) interval 1, (II) interval 2, (III) interval 3, (IV) interval 4, (V) interval 5, (VI) interval 6, (b) Steady-state waveforms of the presented structure in SIDO mode.

the diode D_3 and switch S_3. Diode D_4 is still on, and capacitor C_3 receives energy from the CI secondary side current. A high negative voltage is applied to the LI during this period and its current drops with a high slope. The following equations can be noted for this interval:

$$V_{Lm} = k(V_{C1} - V_{C2} - V_{in2}) \tag{26}$$
$$V_{Lin} = V_{in1} - V_{in2} \tag{27}$$
$$I_{S3} = I_{D3} = I_{Lin} + I_{Lk} \tag{28}$$

Interval 4 (t_4-t_5): At the start of this period, diode D_4 turns off, the only difference between this interval and the previous

period. Switch S_3 and diode D_3 are still on and source V_{in2} is charging by the energy of source V_{in1}. In addition, the capacitor C_2 recycles the energy of the LI. Ultimately, the LI current reaches the MI current. The equations in this time period can be found as follows:

$$V_{Lm} = k(V_{C1} - V_{C2} - V_{in2}) \tag{29}$$
$$V_{Lin} = V_{in1} - V_{in2} \tag{30}$$

Interval 5 (t_5-t_6): In this interval, at the instant t_5, the LI current becomes less than the MI current, and the current I_{Ns} flows in the opposite direction. Thus, diode D_4 is turned off, and the output diode is turned on. The energy of the input V_{in1}, the inductor L_{in}, the secondary side of the CI, and capacitors C_2 and C_3 provide the output load demand. At instant t_6 of this period, the sum of the LI current and the CI secondary side current surpasses the input inductor current. Thus, the current of diode D_1 becomes negative, and it turns off naturally. Equations of this interval can be reported as below:

$$V_o = V_{C1} + V_{C2} - V_{Ns} + V_{C3} \tag{31}$$
$$V_{Lm} = -kV_{C2} \tag{32}$$
$$V_{Lin} = V_{in1} - V_{C1} \tag{33}$$
$$I_{D1} = I_{Lin} - I_{Lk} - I_{Ns} \tag{34}$$

Interval 6 (t_6-t_7): This interval is the last period of the SIDO mode. Like the previous period, the diode D_o is on and transmits energy to the output. This period ends when the switch S_1 turns on. The equations for this interval are as follows:

$$V_o = V_{in1} - V_{Lin} + V_{C2} - V_{Ns} + V_{C3} \tag{35}$$
$$V_{Lm} = k\frac{V_{C1} + kN(V_{C1} - V_{C2}) - V_o}{1 + kN} \tag{36}$$

III. STEADY STATE ANALYSIS OF PROPOSED CONVERTER

A. Voltage gain

Intervals 1 and 4 in DISO mode and intervals 1 and 3 in SIDO mode are too short that they are ignored in the voltage gain calculations. The symbols d_{S1}, d_{S2} and d_{S3} are defined as the switches S_1, S_2 and S_3 Duty cycle, respectively. Due to the simplification of the voltage gain equation of the proposed topology and the similar performance of intervals 5 and 6 in increasing and decreasing slope of charging and discharging energy storage devices, including inductors and capacitors, in both DISO and SIDO modes, intervals 5 and 6 are considered as interval 5. Also, the voltage ripple of capacitors C_1, C_2, and C_3 are ignored. N and k are the turn ratio and the CI coefficient, respectively. The suggested structure has three operating modes, so the voltage gain is calculated in each operational mode. All calculations are in CCM mode.

1) DISO mode: In this mode, both inputs V_{in1} and V_{in2} are involved in transferring energy to the output. Also, the switch S_3 is off. The volt-second balance principle applies to the inductors L_{in} and L_m. The equations of this mode are written below:

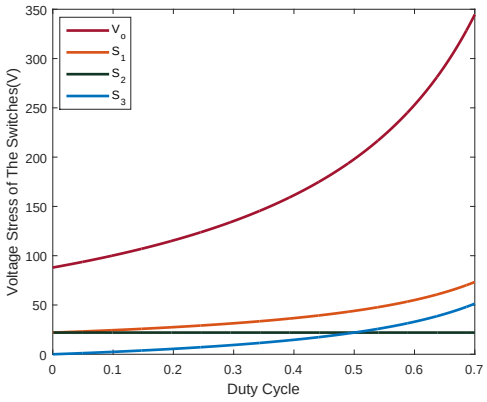


Fig. 5: The MOSFET switches stress voltage of proposed converter in SISO mode (input=$V_{in1} = 22(V)$).

$$V_{C1} = \frac{V_{in1} + d_{S2}V_{in2}}{1 - d_{S1}} \tag{37}$$
$$V_{C2} = d_{S1}V_{C1} = \frac{d_{S1}(V_{in1} + d_{S2}V_{in2})}{1 - d_{S1}} \tag{38}$$
$$V_{C3} = NV_{Lm_{on}} = kN(V_{in1} + d_{S2}V_{in2}) \tag{39}$$
$$V_{Ns} = -kNV_{C2} = -kN\frac{d_{S1}(V_{in1} + d_{S2}V_{in2})}{1 - d_{S1}} \tag{40}$$

according to equations (14) and (37) to (40), the suggested structure voltage gain is calculated as follows:

$$V_o = \frac{1 + kN + d_{S1}}{1 - d_{S1}}(V_{in1} + d_{S2}V_{in2}) \tag{41}$$

Due to the small value of leakage inductance, it can be ignored in calculations. Therefore, $k = 1$, and the voltage gain is as below:

$$V_o = \frac{1 + N + d_{S1}}{1 - d_{S1}}(V_{in1} + d_{S2}V_{in2}) \tag{42}$$

2) SISO mode: In this mode, only one of the sources V_{in1} or V_{in2} transfers energy to output, and both switches S_2 and S_3 are off. The converter voltage gain in this mode can be determined by using the voltage gain calculated in DISO mode, assuming that the S_2 switch is off ($d_{S2} = 0$). according to equation (41), the offered structure voltage gain in SISO mode is written below:

$$V_o = \frac{1 + kN + d_{S1}}{1 - d_{S1}}(V_{in1} \ or \ V_{in2}) \tag{43}$$

Due to the small value of the leakage inductance, it can be ignored. Therefore, $k = 1$, and the voltage gain in SISO mode is as follows:

$$V_o = \frac{1 + N + d_{S1}}{1 - d_{S1}}(V_{in1} \ or \ V_{in2}) \tag{44}$$

3) SIDO mode: In this mode, the source V_{in1} supplies the energy required to charge the storage source V_{in2} and the output demand. The switch S_2 is off in this mode.

The volt-second balance principle applies to the L_{in} and L_m, the equations related to this mode are written below:

$$V_{C1} = \frac{V_{in1} - d_{S3}V_{in2}}{1 - d_{S1} - d_{S3}} \tag{45}$$
$$V_{C2} = \frac{(d_{S1} + d_{S3})V_{in1} - d_{S3}V_{in2}}{1 - d_{S1} - d_{S3}} \tag{46}$$

TABLE I: comparison of similar high voltage-gain multi-port topologies with proposed structure.

Converter	Number of Elements						Voltage Gain of SISO Mode	No. of CCI	No. of IIF	Charging Path of Storage Device	Input Current Ripple
	S	D	C	L	CL	T					
[1]	4	2	3	2	0	11	$1/(1-D)$	2	1	✓	Low
[2]	2	3	4	2	0	11	$1/(1-D)$	2	0	×	Low
[4]	4	2	1	1	0	8	$D/(1-D)$	0	2	✓	High
[33]	4	4	7	0	1	16	$(1+N)/(1-D)$	0	2	✓	High
[34]	5	5	5	0	2	17	$(1+ND)/(1-D)$	0	2	✓	High
[35]	3	5	4	1	1	14	$(1+N)/(1-D)$	0	2	✓	High
[36]	2	8	5	2	0	17	$(1+N)/(1-D)$	2	0	×	Low
[37]	4	5	3	1	0	13	$1/(1-D)$	1	2	✓	High
[38]	2	4	5	2	0	13	$4/(1-D)$	2	2	×	Low
[39]	4	5	9	0	2	20	$(1+N)/(1-D)$	0	2	✓	High
proposed	3	5	4	1	1	14	$(1+N+D)/(1-D)$	2	2	✓	Low

CCI= Continues Current Inputs, IIF= Inputs with Independent Functionality.

$$V_{C3} = NV_{Lm_{on}} = kN(V_{C1} - V_{C2}) = kNV_{in1} \quad (47)$$

$$V_{Ns} = -kNV_{C2} = -kN\frac{(d_{S1}+d_{S3})V_{in1} - d_{S3}V_{in2}}{1-d_{S1}-d_{S3}} \quad (48)$$

according to equations (31) and (45) to (48), the presented structure voltage gain is calculated as follows:

$$V_o = \frac{1}{1-d_{S1}-d_{S3}}((1+kN+d_{S1}+d_{S3})V_{in1} - (2+kN)d_{S3}V_{in2}) \quad (49)$$

Due to the small value of leakage inductance, it can be ignored. Therefore, $k=1$, and the voltage gain is as follows:

$$V_o = \frac{1}{1-d_{S1}-d_{S3}}((1+N+d_{S1}+d_{S3})V_{in1} - (2+N)d_{S3}V_{in2}) \quad (50)$$

B. Voltage stress of switches and diodes

In this part, the switches and diodes voltage stress of the presented topology in all modes are given below:

DISO mode:

$$V_{S1} = V_{D1} = \frac{V_{in1} + d_{S2}V_{in2}}{1-d_{S1}} \quad (51)$$

$$V_{S2} = V_{D2} = V_{in2} \quad (52)$$

$$V_{S3} = V_{D3} = \frac{V_{in1} - (1-d_{S1}-d_{S2})V_{in2}}{1-d_{S1}} \quad (53)$$

$$V_{D4} = \frac{N(V_{in1} + d_{S2}V_{in2})}{1-d_{S1}} \quad (54)$$

$$V_{Do} = \frac{(1+N)(V_{in1} + d_{S2}V_{in2})}{1-d_{S1}} \quad (55)$$

SIDO mode:

$$V_{S1} = V_{D1} = \frac{V_{in1} - d_{S3}V_{in2}}{1-d_{S1}-d_{S3}} \quad (56)$$

$$V_{S2} = V_{in2} \quad (57)$$

$$V_{S3} = V_{D3} = \frac{V_{in1} - (1-d_{S1})V_{in2}}{1-d_{S1}-d_{S3}} \quad (58)$$

$$V_{D2} = 0 \quad (59)$$

$$V_{D4} = \frac{N(V_{in1} - d_{S3}V_{in2})}{1-d_{S1}-d_{S3}} \quad (60)$$

TABLE II: The circuit parameters of the experimental prototype

Parameter	**Symbol**	**Value**
Inputs Voltage	V_{in1}	22V
	V_{in2}	24V
Output Voltage	V_{out}	250V
Output Power	P_{out}	100W
Switching Frequency	f_s	50KHz
Inductor	L_{in}	280uH
Coupled-Inductor	L_m	180uH
	$N(N_S/N_P)$	3(54/18)
Capacitors	C_1, C_2	34uF/100V
	C_3	27uF/100V
	C_o	170uF/280V
Switches	S_1, S_2, S_3	IRFB4110
Diodes	D_1, D_3	MBR10H100CT
	D_2	SR3040PT
	D_4, D_o	HERF1604GA

$$V_{Do} = \frac{(1+N)(V_{in1} - d_{S3}V_{in2})}{1-d_{S1}-d_{S3}} \quad (61)$$

If we apply $d_{S2}=0$ in the voltage stress equations of the presented structure in DISO mode, the voltage stress equations for SISO mode (input=V_{in1}) are obtained. The voltage stress diagram of MOSFET switches compared to output voltage in SISO mode(input=$V_{in1}=22(V)$) is shown in Fig. 5.

IV. COMPARISON

In table I, several high step-up multi-input converters have been compared with the presented structure. This table lists some main features of the multi-input converters, including the number of elements, voltage gain, the number of continuous current inputs, the number of independent inputs, storage device charging path, and input current ripple rate. The presented structure has two independent and continuous current inputs, and the current ripple of the suggested structure inputs is low. Continuous current of inputs is proper for renewable energy

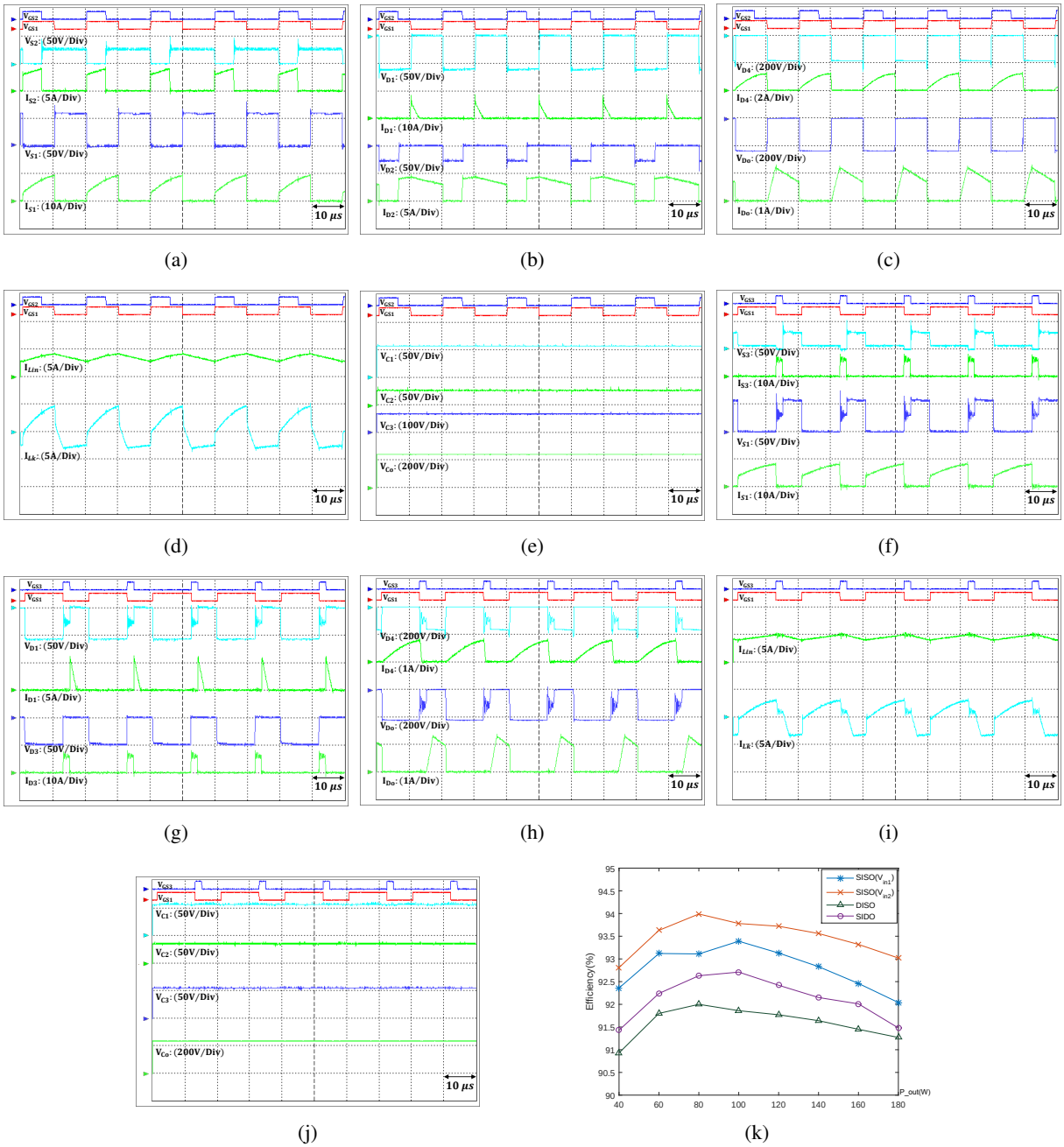


Fig. 6: Experimental waveforms of implemented prototype, (a-e) Voltage and current waveforms of elements in DISO mode, (f-j) Voltage and current waveforms of elements in SIDO mode, (k) The experimental efficiency of proposed structure in all modes.

sources. Also, this structure has a high voltage gain compared to similar topologies and has a path to charge the storage unit. By comparing the converters in this table, it can be inferred that the voltage gain of the suggested topology is higher than all introduced converters by considering N=4. The merits of the proposed converter compared to [4], [33]–[35], [39] is continuous current inputs, and presented structure compared to [1], [2], [36] has two input that can operate independently. Also, the suggested converter compared with [2], [36], [38] has a charging path to charge the storage unit. Fewer active switches make it easier to control the converter and reduce its power loss. The proposed structure, in comparison with [1], [4], [33], [34], [37], [39] has fewer active switches and also, in comparison with [33], [34], [36], [39] has fewer circuit elements that reduce the cost of converter construction. In Fig. 7, the voltage gain of the converters that are compared in table I is investigated.

V. Experimental Results

To confirm the performance of the presented converter, a 100-watt prototype has been designed and implemented. The circuit parameters of the experimental prototype are documented in table II. This converter has two inputs, V_{in1}

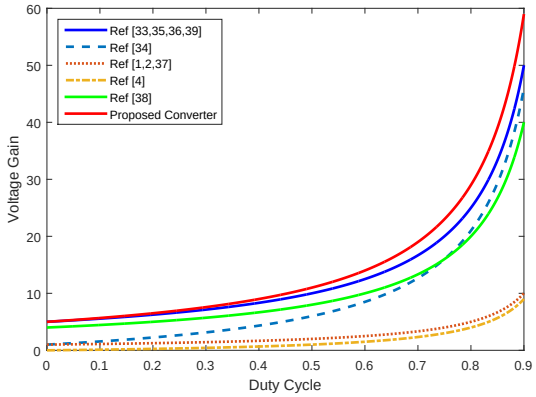


Fig. 7: Voltage gain comparison (N=4).

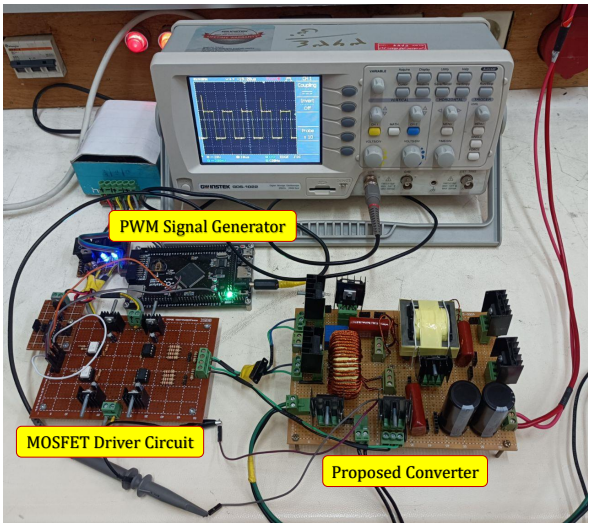


Fig. 8: The implemented prototype photography.

and V_{in2}, which are 22 volts and 24 volts, respectively, and the output voltage V_o is 250 volts with an output load of 600 ohms. A frequency of 50 kHz has been selected to reduce the size of passive elements and manufacturing costs. Also, all diodes are selected from the Schottky model to reduce the forward voltage drop. In the DISO mode, the input V_{in1} cannot independently supply the required output power. Therefore, this source supplies the output power with the support of auxiliary source V_{in2}. Fig. 6a to Fig. 6e show the waveforms of this mode. In SIDO mode, the generated power of source V_{in1} is more than the load requirement. Therefore, the output requirement is satisfied, and part of the energy is stored in the source V_{in2}. Fig. 6f to Fig. 6j illustrate the waveforms of this mode. ARM microprocessor STM32F407ZGT6 is used for producing PWM signals. Mosfet switch IRFB4110 is used for switches S_1, S_2 and S_3. Also, diode MBR10H100CT model is used for diodes D_1 and D_3 and diode SR3040PT model is used for diode D_3. Finally, the diode HERF1604GA model is used for diodes D_4 and D_o. The type of input inductor core is an iron powdered toroid core, and its model number is T130-52. Also, the type of CI is EE 42/21/15 with a 0.4 mm air gap. Experimental results are displayed in Fig. 6. It is noticeable from the figures of the experimental results (Fig. 6) that in both DISO and SIDO modes, the voltage stress of switches S_1, S_2, and S_3 are about 75 volts, 45 volts, and 50 volts, respectively, which is low voltage stress compared to the output voltage. Although the proposed structure is a converter with hard switching condition and the number of elements is high in this topology, the converter has relatively high efficiency. In the design of this converter, the focus has been on lowering the voltage stress of the semiconductors to increase the efficiency of the suggested converter. The efficiency of the presented converter in various output powers and all converter operating modes is illustrated in Fig. 6k.

VI. Conclusion

This document develops a high-gain non-isolated multi-port DC-DC converter for renewable energy sources. The benefits of this structure are having independent and Continuous current inputs, switches with low voltage stress, the energy storage source charging path, and using the minimum number of switches. Also, this topology has a high voltage gain compared to similar structures, which is one of the significant advantages of this topology. The features of this structure are verified by testing a laboratory prototype. The presented structure has three modes, SISO mode, DISO mode, and SIDO mode, and all modes are explained. This converter has two inputs that can operate independently or simultaneously. Also, these two inputs are continuous current and proper for renewable energy sources. Furthermore, the second input V_{in2} is suitable for energy storage sources which can be charged by source V_{in1} through the charging path. If the first source V_{in1} could not supply the output load, the second source V_{in2} participates in providing output demand.

References

[1] T. Jalilzadeh, N. Rostami, E. Babaei, and S. H. Hosseini, "Bidirectional multi-port dc-dc converter with low voltage stress on switches and diodes," *IET Power Electronics*, 02 2020.

[2] A. Deihimi, M. E. Seyed Mahmoodieh, and R. Iravani, "A new multiinput step-up dc–dc converter for hybrid energy systems," *Electric Power Systems Research*, vol. 149, pp. 111–124, 2017.

[3] K. Reddy and D. S. Natarajan, "Energy sources and multi-input dcdc converters used in hybrid electric vehicle applications – a review," *International Journal of Hydrogen Energy*, vol. 43, 08 2018.

[4] S. Athikkal, G. Guru Kumar, K. Sundaramoorthy, and A. Sankar, "A non-isolated bridge-type dc–dc converter for hybrid energy source integration," *IEEE Transactions on Industry Applications*, vol. 55, no. 4, pp. 4033–4043, 2019.

[5] A. Nahavandi, M. T. Hagh, M. B. B. Sharifian, and S. Danyali, "A nonisolated multiinput multioutput dc–dc boost converter for electric vehicle applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1818–1835, 2015.

[6] T. Jalilzadeh, N. Rostami, E. Babaei, and M. Maalandish, "Ultra-stepup dc-dc converter with low voltage stress on devices," *IET Power Electronics*, 10 2018.

[7] S. Haghighian, S. Tohidi, M. R. Feyzi, and M. Sabahi, "Design and analysis of a novel sepic-based multi-input dc/dc converter," *IET Power Electronics*, vol. 10, 05 2017.

[8] Y. Wang, F. Han, L. Yang, R. Xu, and R. Liu, "A three-port bidirectional multi-element resonant converter with decoupled power flow management for hybrid energy storage systems," *IEEE Access*, vol. 6, pp. 61 331–61 341, 2018.

[9] C.-L. Shen and L.-Z. Chen, "Dual-input isolated converter with dualcharge- pump cell for high step-up voltage ratio achievement," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 11, pp. 9383–9392, 2020.

[10] V. Karthikeyan and R. Gupta, "Multiple-input configuration of isolated bidirectional dc–dc converter for power flow control in combinational battery storage," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 1, pp. 2–11, 2018.

[11] H. Wu, K. Sun, L. Zhu, and Y. Xing, "An interleaved half-bridge three-port converter with enhanced power transfer capability using three-leg rectifier for renewable energy applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 606–616, 2016.

[12] A. Alhatlani and I. Batarseh, "Review of partially isolated three-port converters for pv-battery systems that interface a pv, bidirectional battery, and load," in 2019 *IEEE Conference on Power Electronics and Renewable Energy (CPERE)*, 2019, pp. 465–472.

[13] S. Rostami, V. Abbasi, and M. Parastesh, "Design and implementation of a multiport converter using z-source converter," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 10, pp. 9731–9741, 2021.

[14] S. Athikkal, K. Sundaramoorthy, and A. Sankar, "Development and performance analysis of dual-input dc-dc converters for dc microgrid application: Dual input dc-dc converters for dc microgrid application," *IEEJ Transactions on Electrical and Electronic Engineering*, vol. 13, 03 2018.

[15] G. Guru Kumar, K. Sundaramoorthy, S. Athikkal, and V. Karthikeyan, "Dual input superboost dc–dc converter for solar powered electric vehicle," *IET Power Electronics*, vol. 12, no. 9, pp. 2276–2284, 2019.

[16] C. Balaji, S. S. Dash, N. Hari, and P. C. Babu, "A four port non-isolated multi input single output dc-dc converter fed induction motor," in 2017 *IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*, 2017, pp. 631–637.

[17] G. Chen, Y. Liu, X. Qing, M. Ma, and Z. Lin, "Principle and topology derivation of single-inductor multi-input multi-output dc–dc converters," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 1, pp. 25–36, 2021.

[18] S. A. Yasin, J. Kumar, Y. Kumar, S. Athikkal, and J. Peter, "Analysis of a dual input dc-dc converter topology based on sepic configuration," in *2019 International Conference on Power Electronics Applications and Technology in Present Energy Scenario (PETPES)*, 2019, pp. 1–6.

[19] M. Chen, F. Gao, R. Li, and X. Li, "A dual-input central capacitor dc/dc converter for distributed photovoltaic architectures," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 305–318, 2017.

[20] R. R. Ahrabi, H. Ardi, M. Elmi, and A. Ajami, "A novel step-up multiinput dc–dc converter for hybrid electric vehicles application," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3549–3561, 2017.

[21] F. Kardan, R. Alizadeh, and M. R. Banaei, "A new three input dc/dc converter for hybrid pv/fc/battery applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1771–1778, 2017.

[22] K. Varesi, H. Hosseini, M. Sabahi, E. Babaei, and N. Vosoughi kurdkandi, "Performance and design analysis of an improved non-isolated multiple input buck dc/dc converter," *IET Power Electronics*, vol. 10, 03 2017.

[23] X. L. Li, Z. Dong, C. K. Tse, and D. D.-C. Lu, "Single-inductor multi-input multi-output dc–dc converter with high flexibility and simple control," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 104–13 114, 2020.

[24] L. Yu and H. Wang, "A novel dual-input zvs dc/dc converter for lowpower energy harvesting applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 1197–1206, 2019.

[25] B. L.-H. Nguyen, H. Cha, T.-T. Nguyen, and H.-G. Kim, "Family of integrated multi-input multi-output dc-dc power converters," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018, pp. 3134–3139.

[26] F. Akar, Y. Tavlasoglu, E. Ugur, B. Vural, and I. Aksoy, "A bidirectional nonisolated multi-input dc–dc converter for hybrid energy storage systems in electric vehicles," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 10, pp. 7944–7955, 2016.

[27] K. Varesi, S. H. Hosseini, M. Sabahi, and E. Babaei, "Modular nonisolated multi-input high step-up dc-dc converter with reduced normalized voltage stress and component count," *IET Power Electronics*, vol. 11, 01 2018.

[28] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of highstep-up coupled-inductor boost converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 689–704, 2016.

[29] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up dc–dc converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143–9178, 2017.

[30] L. Schmitz, D. C. Martins, and R. F. Coelho, "Generalized high stepup dc-dc boost-based converter with gain cell," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 2, pp. 480–493, 2017.

[31] F. Akar, "A high-efficiency bidirectional non-isolated multi-input converter," in *2016 19th International Symposium on Electrical Apparatus and Technologies (SIELA)*, 2016, pp. 1–4.

[32] E. Babaei and O. Abbasi, "Structure for multi-input multi-output dc–dc boost converter," *IET Power Electronics*, vol. 9, 08 2015.

[33] V. R. Teja, S. Srinivas, and M. K. Mishra, "A three port high gain nonisolated dc-dc converter for photovoltaic applications," in *2016 IEEE International Conference on Industrial Technology (ICIT)*, 2016, pp. 251–256.

[34] R. Faraji, H. Farzanehfard, G. Kampitsis, M. Mattavelli, E. Matioli, and M. Esteki, "Fully soft-switched high step-up nonisolated threeport dc–dc converter using gan hemts," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8371–8380, 2020.

[35] R. Faraji and H. Farzanehfard, "Fully soft-switched multiport dc–dc converter with high integration," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1901–1908, 2021.

[36] R. Faraji, E. Adib, and H. Farzanehfard, "Soft-switched non-isolated high step-up multi-port dc-dc converter for hybrid energy system with minimum number of switches," *International Journal of Electrical Power & Energy Systems*, vol. 106, pp. 511–519, 2019.

[37] B. Zhu, Q. Zeng, D. Vilathgamuwa, Y. Li, and X. She, "Non-isolated high voltage gain dual-input dc/dc converter with zvt auxiliary circuit," *IET Power Electronics*, vol. 12, pp. 861–868, 04 2019.

[38] T. Cheng, D. D.-C. Lu, and L. Qin, "Non-isolated single-inductor dc/dc converter with fully reconfigurable structure for renewable energy applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 3, pp. 351–355, 2018.

[39] B. P. Baddipadiga and M. Ferdowsi, "A high-voltage-gain dc-dc converter based on modified dickson charge pump voltage multiplier," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7707–7715, 2017.

[40] R. Faraji and H. Farzanehfard, "Soft-switched nonisolated high step-up three-port dc–dc converter for hybrid energy systems," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 101–10 111, 2018.

Seyyed Mojtaba Taheri was born in 1996, in Rasht, Iran. He received his Bachelor's degree in electrical engineering from the University of Guilan, Rasht, Iran, in 2018 and his Master's degree in electrical engineering from the University of Guilan, Rasht, Iran, in 2021. His main research interests are designing and implementing multi-port topologies, renewable energy technologies and applications, and Hybrid and electric vehicles.

Alfred Baghramian received his Bachelor's degree in electrical engineering in 1991 from the Isfahan University of Technology, Isfahan, Iran, his Master's degree in electrical engineering in 1994 from the Tarbiat-Modarres University, Tehran, Iran, and his PhD degree in power electronics in 2006 from the Birmingham University, Birmingham, UK. His study interests are analysis, modeling, and controlling power electronic circuits. Dr. Alfred Baghramian is an associate professor. Since 1994, he has been working at the Guilan University, Rasht, Iran.

Seyed Amir Pourseyedi was born in Rasht, Iran. He received his B.S. degree in electrical engineering from the University of Guilan, Rasht, Iran, in 2018, and his M.S. degree in electrical engineering from the University of Guilan, Rasht, Iran, in 2021. His research interests include designing and controlling power electronic converters, high-efficiency power converters, and high step-up dc-dc converters.