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A New Structure of Single-Switch Ultra High-Gain DC/DC Converter for Renewable Energy Applications

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Abstract— **This study introduces a new modified high gain single-switch SEPIC-based DC/DC converter. The low input ripple of the proposed converter makes it very suitable for renewable energy applications. In the proposed topology, a three-winding coupled-inductor and a voltage doubler rectifier are used to achieve high voltage gain without needing an extreme duty cycle. This circuit can provide an ultra-high voltage conversion ratio without requiring a large number of the turns ratio of the Three-Winding Coupled-Inductor (TWCI). Due to a regenerative clamped circuit, the leakage energy of the coupled-inductor is recycled; thus, the maximum voltage spike across the single power switch is restricted. Therefore, MOSFET with a low maximum voltage rating can be utilized, which can alleviate the conduction power dissipations of the converter. Here, the switching power losses have been reduced significantly due to the circuit's soft-switching operation for the switch and all diodes. The steady-state analysis of the proposed converter are discussed thoroughly. Finally, the theoretical analysis is verified through the experimental results from a sample prototype (200 W, 30 V-250 V).**

NOMENCLATURE

D	Duty cycle of the main switch
f_s	Switching frequency
f_R	Resonant frequency
LRR	Low Reverse Recovery
TWCI	Three-Winding Coupled-Inductor
CI	Coupled-Inductor
VM	Voltage Multiplier
ZCS	Zero Current Switching
3D	Three-Dimensional
SEPIC	Single-Ended Primary-Inductor Converter
RES	Renewable Energy Sources
CCM	Continuous Conduction Mode
RMS	Root Mean Square

I. INTRODUCTION

In the past few decades, environmental consequences of consuming fossil fuels and decreasing their reserves have made it requisite to utilize renewable energy sources (RES) such as Fuel cells, PV, and wind energy. Due to the limited voltage of these sources (20-30V), it is imperative to use step-up (High-gain) switch-mode DC-DC converters as an interface circuit to reach a regulated high DC output voltage. Some applications of such converters are energy harvesting, medical devices, lighting systems, and portable devices. The specific requirements of these circuits are high voltage conversion ratio, low voltage/current stress, enough high efficiency, and compact design [1]. Moreover, drawing non-pulsating current from RES-connected converters is also essential, as a high current ripple can lead to decreasing the proper performance, including power density and reliability [1, 2]. Because of higher power density and lower costs, non-isolated structures of step-up converters are often favored for low-power applications.

With the help of different voltage boosting techniques, including Voltage Multipliers (VMs) cells/rectifiers, switched capacitors/switched inductors, and multi-stage/level [1, 3, 4], many high gain converters have been introduced. Nevertheless, these converters often provide high voltage gain under hard-switching conditions and many components, compromising their proper performance.

To improve the performance of such converters, using magnetically devices in the form of Coupled-Inductor (CI) or Built-In Transformer are a good solution for high gain applications. Flexible structure and simple adjustment of turns ratio are the main merits of these techniques[3, 5]. However, because of the leakage energy of CI, a huge voltage spike exists across the switching devices. However, this voltage spike can be eliminated by using active or passive clamp circuits [6, 7]. It is noteworthy that hard-switching performance and diode reverse recovery issues are the main obstacles of high gain circuits to reach a decent efficiency.

In recent years, various coupled-inductor-based step-up converters with acceptable performance have been introduced to process power from the low-voltage DC side to the high-voltage DC side. In step-up DC-DC converters [8-10], CI and VM circuits have been combined. Although offering high static DC Voltage levels, high input current ripple is the main drawback of these converters, which limits their applications for RESs. Some CI-based ultra high-gain converters with low voltage stress across the switching devices are presented in [11, 12]. Despite the very high voltage gain under the soft-switching performance, the input current is not smooth. Converters with continuous input current and low ripple are useful for RES applications [13-16], which is desirable for the battery, fuel cell and PV applications. In these circuits, the single power switch and all diodes operate under ZCS and Low Reverse Recovery (LRR) issues, respectively. Even so, the voltage conversion ratio of these converters is not large enough. Also, a high step-up boost-based DC/DC converter with a built-in transformer and an active clamp is suggested in [17]. Nevertheless, the use of two active switches is the main limitation of the mentioned topology. Moreover, two new types of zero voltage switching step-up converters with low input current ripple are presented in [18, 19]. The presented converters provide high voltage gain and low voltage stress across the main power switch. But, the use of two active switches and many components are the main demerits of the circuits.

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Recently, step-up DC-DC converters have been introduced in which the voltage gain ratio has the Transe-inverse (or Partial Transe-inverse) characteristic. So that, the voltage gain is increased by decreasing its magnetic turns ratio, which leads to more efficiency improvement. In [20, 21], structures have been proposed to provide high voltage gain coefficients at a lower number of turns ratios than other conventional converters. Nonetheless, high input current ripple (for [20]) and the use of two active switches (for [21]) are the disadvantages of the mentioned topologies, which complicate the gating circuit. In addition, a new high step-up trans-inverse DC/DC converter with a continuous current form is proposed in [22]. However, hard-switching performance along with high reverse recovery problems are disadvantages of the converter.

Furthermore, using a Three-Winding Coupled-Inductor (TWCI) makes it possible to meet a more flexible on voltage conversion ratio and other performance indicators of converter. New types of single-switch TWCI-based high gain converters with soft-switching performance and LRR issues are suggested in [23-25]. Although high voltage gain, these converters suffer from the high input current ripple, which negatively affects the fuel cell stacks. To solve this problem, in [26-28], three new types of TWCI–based step-up DC-DC topologies with low input current ripple and regenerative passive clamp capacitor are presented. In these single-switch circuits, the leakage inductors of the windings of the TWCI help to eliminate the diodes' reverse recovery challenge. The possibility of meeting high voltage gains under a low number of turns ratios is unique merit of the mentioned circuits. Even so, for these circuits, diodes with very high breakdown voltage are needed. In addition, in [29], using a TWCI, a new single-switch ultra-high voltage gain converter with low input current ripple and voltage stress is suggested. However, this converter lacks the trans-inverse feature. So that higher voltage gains are obtained under more turns ratios of the TWCI. In addition, a new quadratic step-up converter based on TWCI is suggested in [30]. although a high voltage gain, this converter suffers from hard switching performance.

This paper introduces a new single-switch ultra-high step-up DC-DC converter with low steady voltage stress and low input current ripple to solve the problems mentioned above. A TWCI and a voltage doubler rectifier are integrated into the proposed converter to reach an ultra-high voltage conversion ratio. The unique property of the proposed circuit is the possibility of achieving higher voltage gains at a lower number of turns ratio of the coupled-inductor. The single power switch operates at ZCS conditions with low voltage stress. Furthermore, considering a resonant tank using the leakage inductor and the middle capacitors of the circuit, the magnitude of the turn-off current of the switch can be alleviated considerably. Besides, due to full soft-switching performance for all components, the reversed-recovery procedures of the diodes are eliminated. These benefits provide enough high efficiency for the introduced converter.

This paper is organized as follows: the topology description and steady-state analysis are provided in Sections II and III. In Section IV, the advantages of the introduced circuit are compared with other similar topologies. Section V presents experimental results. Eventually, conclusions are drawn in Section VI.

II. TOPOLOGY AND OPERATING PRINCIPLE

The power circuit of the introduced topology is depicted in Fig. 1. The proposed topology is a type of modified structure of the conventional SEPIC. This converter is formed by an input inductor (L_{in}), a TWCI (with turns ratios N_1, N_2, and N_3), a single power switch, five diodes, and six capacitors. The loops C_1-N_2-N_1-D_c, and $D_{1\text{-}3}$-$C_{2\text{-}3}$-N_3, have a VM role to enhance the voltage gain. A regenerative passive clamp circuit (C_c and D_c) limits the maximum steady voltage rate across the power switch. Adopting a resonant circuit among the capacitors C_1, C_c, and the primary and the secondary sides (N_1 and N_2) of the

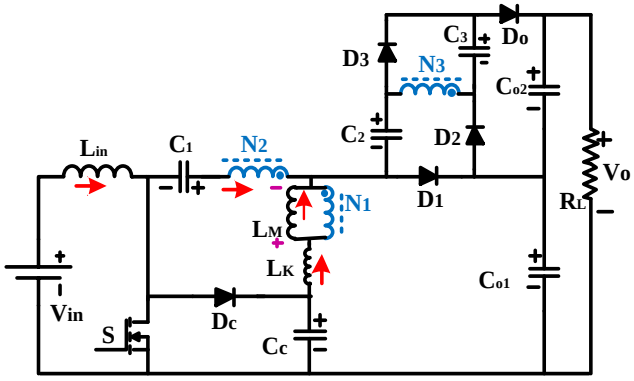


Fig. 1. The proposed topology.

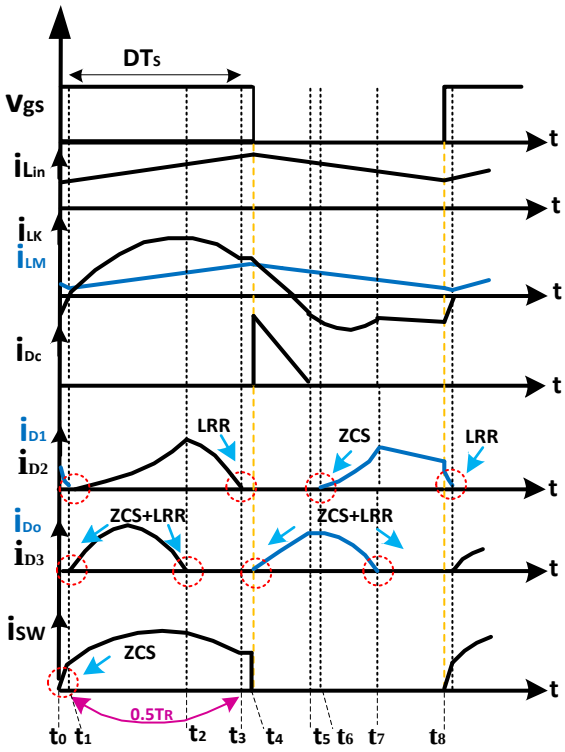


Fig. 2. The Key waveforms.

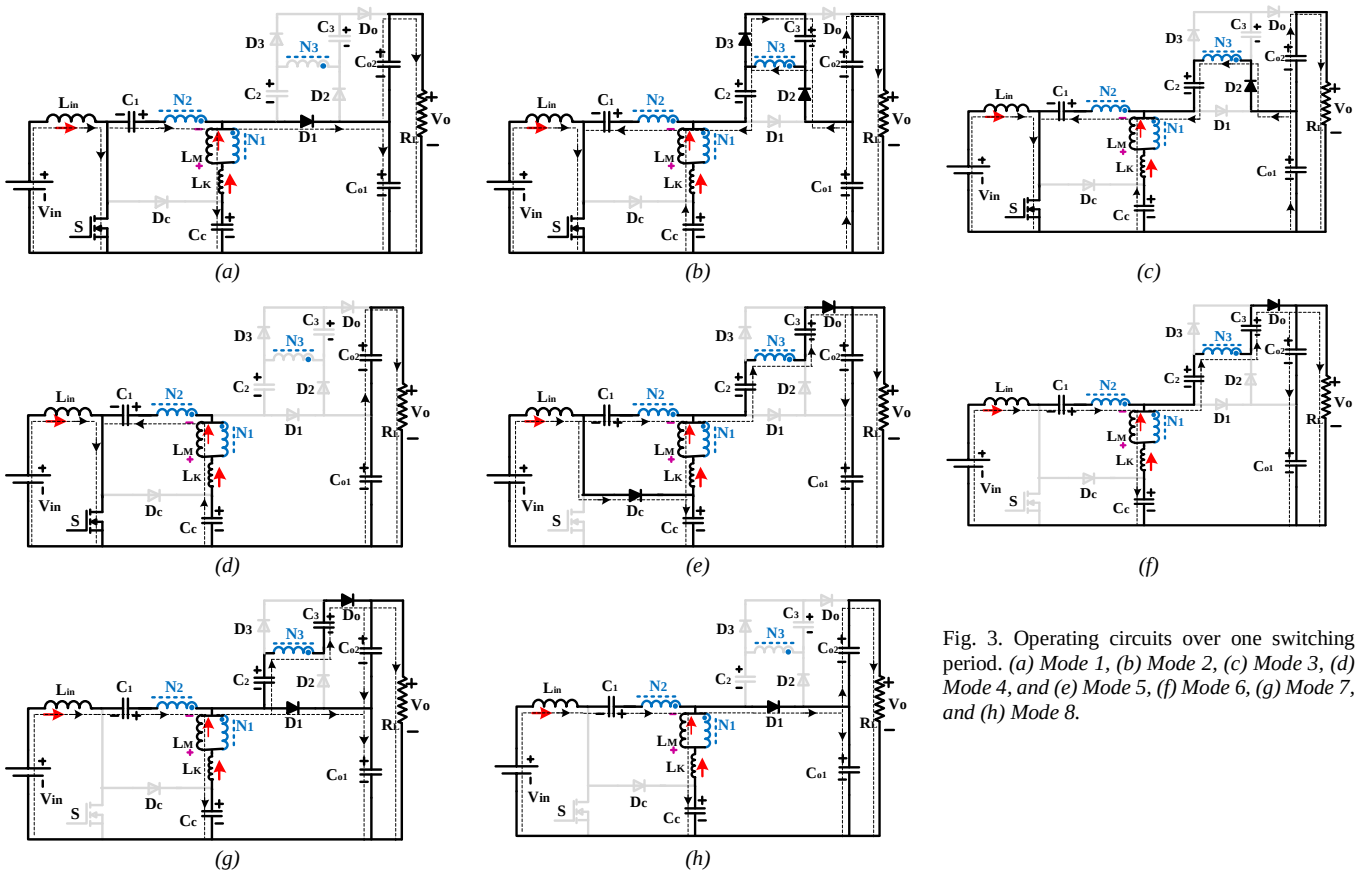


Fig. 3. Operating circuits over one switching period. *(a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, and (e) Mode 5, (f) Mode 6, (g) Mode 7, and (h) Mode 8.*

TWCI leads to the currents of the switch and the diodes D_2 and D_3 change as a sinusoidal form. The result is a reduction of the switching and reverse recovery issue. To simplify the proposed circuit analysis in CCM, the voltages on the capacitors are assumed to be a constant value. Moreover, the TWCI is modeled as an ideal transformer with a parallel magnetizing inductor (L_M) and a merged leakage inductor (L_k). Fig. 2 shows the typical key waveforms of the introduced converter. Also, operating circuits over one switching period are presented in Fig. 3.

Mode 1 [t_0 - t_1]: The switch begins to conduct at ZCS conditions in this interval. As it is shown in Fig. 3 (a), D_1 is also conducting, while other diodes are in reverse bias condition. During this short time interval, the input inductor begins to receive energy from the source V_{in}, thus its current increase linearly. Also, the clamp capacitor C_c receives energy from the primary side of the TWCI. The current of D_1 reaches zero under the LRR conditions at the end of this short operating mode.

Mode 2 [t_1 - t_2]: In the second time interval, the single power switch remains ON, while the diodes D_2 and D_3 start to conduct under the ZCS feature. Similar to the first mode, the input inductor L_{in} received energy from the input voltage. The capacitor C_3 receives energy from the tertiary side of the TWCI. Since the positive voltage is applied to L_M, its current is increased linearly. During this interval, to decrease the switch current magnitude at the turn-off instant, a resonant circuit among the primary and secondary sides of the TWCI and also the capacitors C_c and C_1 can be adopted. Regarding Fig.3 (b), this resonant helps to change the current waveform of the main switch is changed as a sinusoidal form. Hence, it can alleviate the switching power dissipation. The resonant frequency of the circuit is derived as:

$$f_R = \frac{1}{T_R} = \frac{1}{2\pi\sqrt{L_{k1}\left[\left(\frac{2n_{21}.n_{31}+1}{2n_{31}+1}C_1\right)\middle\|C_c\right]}} \quad (1)$$

Here, $n_{21}=N_2/N_1$ and $n_{31}=N_3/N_1$. For better performance, the half of resonant period should be close to switching period ($0.5T_R \approx DT_S$). In this mode, the following equations can be given:

$$v_{L_{in}} = V_{in} \quad (2)$$

$$v_{LM} = \frac{v_{Cc}-v_{C1}}{1-n_{21}} \quad (3)$$

$$v_{C3} = n_{31}v_{LM} \quad (4)$$

$$v_{C2} = v_{co1} + v_{C3} - v_{Cc} - v_{LM} \quad (5)$$

Furthermore, the current passed through the power switch is given as:

$$i_s = i_{in} + i_{N2} \quad (6)$$

This mode is finished when the current of D_3 meets zero naturally under a slow slope with LRR.

Mode 3 [t_2 - t_3]: From Fig. 3 (c), only the power switch and the diode D_2 conduct during this short interval. Also, the leakage inductance of the TWCI makes the current of D_2 tend to zero with a slight slope.

Mode 4 [t_3 – t_4]: In continuation of the previous mode, the single power switch is still ON. As shown in Fig. 3 (*d*), the current passed through the secondary side (i_{N2}) and the leakage inductor of the TWCI are identical. Moreover, the current of the secondary side of the TWCI charges the balancing capacitor C_1 of the converter. In this mode, the current of the switch is derived as follow:

$$i_S = i_{in} + i_{LK} \quad (7)$$

Mode 5 [$t_4 - t_5$]: According to Fig. 3 (e), the single power switch is turned OFF at $t = t_4$. Meanwhile, the diode D_c starts to conduct simultaneously; thus, the voltage across the switch is clamped. The leakage inductor of the tertiary side and the capacitors C_2 and C_3 in series transfer their energies to the output capacitors C_{o1} and C_{o2}. Moreover, during this mode, the clamp capacitor C_c receives energy from L_{in}. Hence, the currents of the input and the magnetizing inductors begin to decrease linearly. This operating mode is ended when D_c turns OFF with the LRR feature. The following equations can be achieved in this mode:

$$v_{Lin} = V_{in} - v_{Cc} \quad (8)$$

$$v_{LM} = \frac{-v_{C1}}{1-n_{21}} \quad (9)$$

$$v_{Co2} = v_{Cc} + (1+n_{31})v_{LM} + v_{C2} + v_{C3} - v_{Co1} \quad (10)$$

Mode 6 [$t_5 - t_6$]: The output diode D_o is still ON during this small interval. Same as the previous mode, the output capacitors receive energy from the TWCI and the capacitors C_2 and C_3 in series. At $t=t_6$, the diode D_1 starts to conduct under ZCS conditions.

Mode 7 [$t_6 - t_7$]: As it is depicted in Fig. 3 (*g*), the energies of the tertiary side of the coupled inductor along with the capacitors C_2 and C_3 are delivered to the second output capacitor C_{o2}. Meanwhile, the first output capacitor C_{o1} receives energy from the primary and secondary sides through the diode D_1. This operating mode is ended when the current of D_o reaches zero at $t = t_7$ at the LRR. During this state, the voltage loop equations are as follows:

$$v_{co1} = v_{Cc} + v_{C3} - v_{LM} \quad (11)$$

$$v_{co2} = v_{C2} + v_{C3} - n_{31}v_{LM} \quad (12)$$

Mode 8 [$t_7 - t_8$]: In this mode, D_1 is conducting, and other diodes are blocking. Regrading Fig. 3 (*g*), the energies stored in the input and magnetizing inductors are released to the first output capacitor C_{o1}.

III. Steady-State Analysis

In this part, the steady-state analysis of the introduced topology is carried out. To simplify the analysis, the effect of the leakage inductor and the short time intervals can be neglected.

A. Voltage Conversion Ratio

By applying the volt-second balance principle on L_{in} and L_M, the average voltages of C_c and C_1 are derived as follows:

$$V_{Cc} = \frac{V_{in}}{1-D} \quad (13)$$

$$V_{C1} \approx \frac{D.V_{in}}{1-D} \quad (14)$$

Using (3), (4), (13), and (14), the voltage of the capacitor C_3 is determined as:

$$V_{C3} = \frac{n_{31}}{(1-n_{21})}.V_{in} \quad (15)$$

Also, by re-applying the volt-second balance principle on the input inductor over one switching period and using (2) and (11), the average voltage across the first output capacitor C_{o1} is derived as:

$$V_{Co1} = \frac{1+D-n_{21}}{(1-n_{21})(1-D)}.V_{in} \quad (16)$$

The voltage across the capacitor C_2 can be given with the help of (3) and (5), (15) and (16) as:

$$V_{C2} = \frac{1+n_{31}(1-D)}{(1-n_{21})(1-D)}.V_{in} \quad (17)$$

By substituting (9), (13), (15)-(17) into (10), the average voltage on the second output capacitor C_{o2} is equal to (18).

$$V_{Co2} = \frac{1+n_{31}(2-D)}{(1-n_{21})(1-D)}.V_{in} \quad (18)$$

Eventually, Regarding the proposed converter configuration, the output voltage equals the sum of V_{Co1}, V_{Co2}. Thus, the voltage gain of the proposed converter in CCM is derived from (20) as follow:

$$M = \frac{V_o}{V_{in}} = \frac{2+D+n_{31}(2-D)-n_{21}}{(1-n_{21})(1-D)} \quad (20)$$

To have a clearer picture of the influence of the parameters n_{21} and n_{31} on the voltage conversion ratio (20) of the converter, several curves of the DC Voltage gain as a function of the duty cycle are depicted in Fig. 4. Moreover, Fig. 5 illustrates a *3D* plot of the theoretical voltage versus n_{21} and n_{31} for *D=0.3*, *D=0.55*, and *D=0.75*. Regarding these figures, the voltage gain of the presented topology can be easily adjusted in a wide range with a slight increase in the parameter n_{21} towards unity. Therefore, higher output DC voltage can provide at fewer turns ratios of the TWCI, which alleviates ohmic power dissipations in the windings.

B. Voltage and Current Stress analysis

Based on the upper analysis, the voltage stresses of the switch and the diodes (D_c, D_1, D_2, D_3 and D_o) are obtained as:

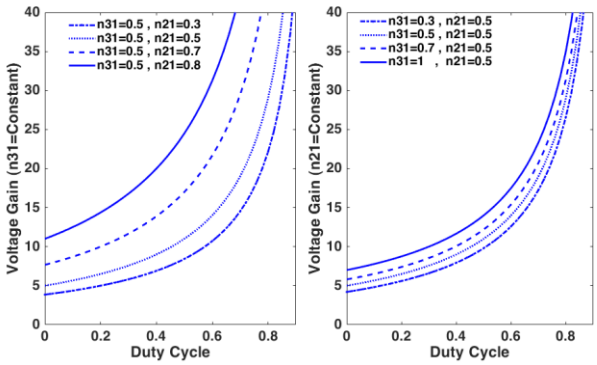


Fig. 4. Ideal DC Voltage gain of the suggested topology versus the duty cycle for different turns ratios.

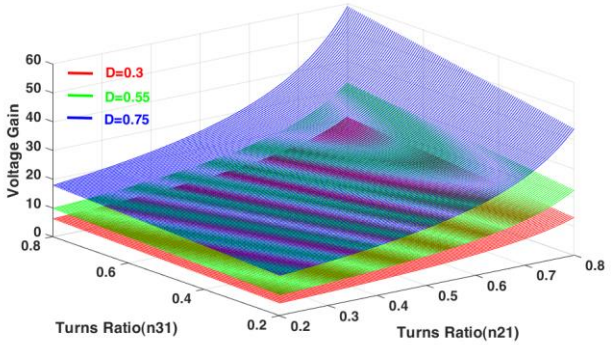


Fig. 5. *3D* plot of the voltage gain as a function of n_{21} and n_{31} under several duty cycles.

$$V_{S(Peak)} = V_{Dc(Peak)} = \frac{V_{in}}{1-D} = \frac{1-n_{21}}{2+D+n_{31}(2-D)-n_{21}} V_o \quad (21)$$

$$V_{D1} = \frac{V_o}{2+D+n_{31}(2-D)-n_{21}} \quad (22)$$

$$V_{D2} = \frac{1+n_{31}}{2+D+n_{31}(2-D)-n_{21}} V_o \quad (23)$$

$$V_{D3} = \frac{n_{21}(1-D)+n_{31}D}{2+D+n_{31}(2-D)-n_{21}} V_o \quad (24)$$

$$V_{Do} = \frac{1+n_{31}(1-D)}{2+D+n_{31}(2-D)-n_{21}} V_o \quad (25)$$

The variation of component voltage stress versus the duty cycle is shown in Fig.6 (n_{21}=n_{31}=0.65). According to this figure, the highest and lowest voltage stresses are applied to the diode D_2 and the power switch respectivily. However, as the duty cycle increases, the value of voltage stresses is decreased.

Based on (21)-(25), steady voltage rates across the switching semiconductors are significantly smaller than the output voltage. Using (6), the peak and RMS values of the switch current are given as:

$$I_{S(Peak)} \approx \left(M + \frac{(1-n_{31})+\frac{\pi}{2D}(2n_{31}+1)}{1-n_{21}}\right) I_o \quad (26)$$

$$I_{S(RMS)} = I_o \sqrt{DX_1^2 + \frac{DX_2^2}{2} + \frac{4DX_1X_2}{\pi}} \quad (27)$$

Here, M is the voltage gain ratio of the proposed topology, and parameters X_1 and X_2 are defined as:

$$X_1 = M + \frac{1-n_{31}}{1-n_{21}} \quad , X_2 = \frac{\pi}{2D}\left(\frac{2n_{31}+1}{1-n_{21}}\right) \quad (28)$$

According to the operating Mode 4, the switch current value at the turn-off instant ($t = t_4$) is equal to (29).

$$i_S^{t=off} = \left(M + \frac{1-n_{31}}{1-n_{21}}\right) I_o \quad (29)$$

Besides, the maximum current magnetude passed from D_c at $t=t_4$ is expressed as follow:

$$i_{Dc(peak)} = i_{SW}^{t=off} \quad (30)$$

Considering the sine changes of the current shape of D_2 and D_3, the peak current magnitude of the mentioned diodes can be determined as:

$$i_{D2_{peak}} = i_{D3_{peak}} \approx \frac{\pi}{2D} I_o \quad (31)$$

Here I_o is the output load current. Furthermore, the maximum current values of D_1 and D_o are approximated as:

$$i_{D1(peak)} \approx \frac{I_o}{1-D-D_5} \quad (32)$$

$$i_{Do(peak)} \approx \frac{M(1-n_{21})+1-n_{31}}{1+n_{31}} I_o \quad (33)$$

where D_5 represents the time duration of the operating Modes 5 and given as:

$$D_5 = \frac{2}{i_{Dc(peak)}} I_o \quad (34)$$

Fig. 7 shows the maximum current value of the switching components as a function of duty cycle at n_{21} = 0.4, n_{31} = 0.35. According to this figure, the duty cycle range 0.35<D<0.65 is the most appropriate range for proper performance.

C. Efficiency Analysis

In practice conditions, the parasitic components of the circuit elements make conduction power losses. Consequently, the efficiency of the converter is affected by conduction dissipations. In this part, to analyze the efficiency of the presented converter, parasitic components are considered, which are summarized in Table I. Also, Fig.8 shows the simplified circuit schematic for analyzing conduction losses

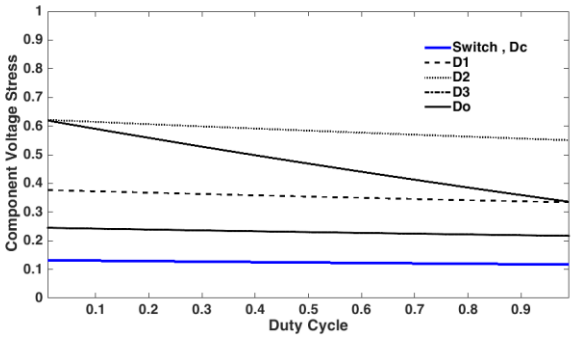


Fig.6. Variation of Component Voltage Stress as a function of the duty cycle.

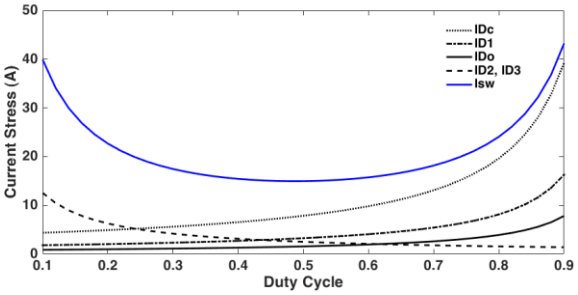


Fig. 7. Maximum current value across the switching components of the proposed circuit.

in the proposed converter.

The ZCS operation of the converter eliminates the switch turn-on power loss. Moreover, the resonant performance in the second operating mode reduces the switch-off power dissipation. Thus, the power loss of the converter switch is calculated as:

$$P_S = \frac{1}{2T_s} . V_{DS}\left(i_S^{t=off} . t_{off}\right) + \frac{1}{2T_s}\left(C_{oss} . V_{DS}^2\right) + R_{DS(on)} . I_{S(RMS)}^2 \quad (35)$$

Following Section II mentioned above, the soft-switching operation for all diodes eliminates the reverse recovery problem. Therefore, the diode conduction losses are obtained as:

$$P_{Di} = V_F . I_{D(AVG)} + r_D . I_{D(RMS)}^2 \quad (36)$$

Also, the capacitors' conduction power losses are calculated as given in (37).

$$P_{Cap.i} = r_{Ci} . I_{C(RMS)}^2 \quad (37)$$

Moreover, the magnetic power losses can be calculated as presented below:

$$P_{Mag.} = r_{L_{in}} . I_{L_{in}(RMS)}^2 + r_{eq} . I_{lk1(RMS)}^2 + P_{Core(Lin,TWCI)} \quad (38)$$

The total power loss of the proposed converter is determined as:

$$P_{Loss} = P_{SW} + P_D + P_{Cap.} + P_{Mag.} \quad (39)$$

The proposed converter efficiency as well as the Non-Ideal voltage gain can be calculated as:

$$\eta = \frac{P_{Out}}{P_{Out}+P_{Loss}} \quad (40)$$

$$M_{Non-Ideal} = \frac{V_o}{V_{in}} = \frac{2+D+n_{31}(2-D)-n_{21}}{(1-n_{21})(1-D)} . \eta \quad (41)$$

The effect of the parasitic components (listed in Table I) on the output voltage gain along with the theoretical efficiency are illustrated in Fig. 9. The main parameters of the proposed converter are considered as: V_{in} = 25 V, R_L = 400 Ω, n_{21}=0.62, n_{31}=0.8, and f_s = 60 kHz. Also, the values of the parasitic components (based on the prototype specifications) of the

TABLE I. THE MAIN PARASITIC PARAMETERS OF THE CIRCUIT ELEMENTS

Parameter	Description
r_{DS}	Static ON-state resistance of the power MOSFET
t_{on} , t_{off}	Turn-off and turn-on transition times of the MOSFET
T_s	The switching cycle time
C_{oss}	Output capacitance of the MOSFET
r_{Ci}	Equivalent Series Resistance (ESR) of the capacitor
V_F	Threshold voltage of the diode
r_D	Conduction resistance of the diode
r_{Lin}, r_{eq}	Series resistances of the input inductor and TWCI

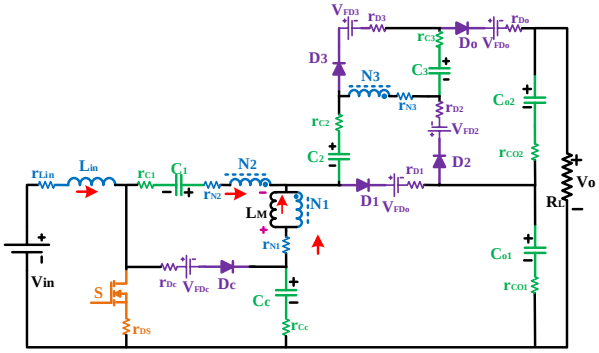


Fig.8. Simplified circuit schematic for analyzing conduction losses in the proposed converter.

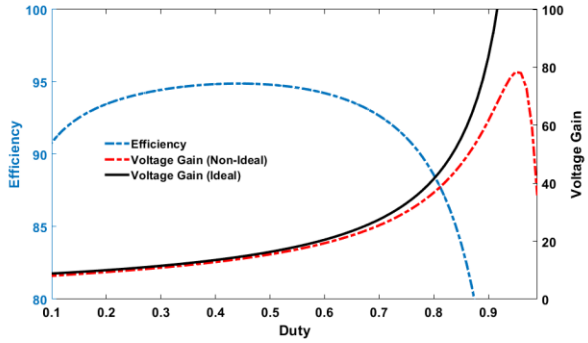


Fig. 9. Voltage gain (Ideal and Non-Ideal) and efficiency of the proposed converter versus duty cycle (f_S=60 kHz and R_L=400 Ω, V_{in}=25V).

circuit are : r_{DS}=3.7mΩ, t_{off}=88ns, C_{oss}=670pF, r_{Cc}=7.1mΩ, r_{C1}=7mΩ, r_{C2}=10mΩ, r_{C3}=10mΩ, r_{Co1}=70mΩ, r_{Co2}=0.1Ω, V_{FDc}=0.6V, V_{FD1}=0.7V, V_{FD2}=0.71V, V_{FD2}=0.7V, V_{FD2}=0.72V, r_{Dc}=3mΩ, r_{D1}=8mΩ, r_{D2}=6.5mΩ, r_{D3}=7mΩ, r_{Do}=12.5mΩ, r_{Lin}=10mΩ, r_{N1}=35mΩ, r_{N2}=10mΩ, r_{N3}=50mΩ). Regarding this figure, due to the high voltage and current levels at higher duty cycles, the maximum power-handling capability and actual voltage are limited, which also happens in other step-up topologies. However, converters such as the proposed converter, which have a high voltage gain, and soft-switching performance, can provide higher power-handling capacities and voltage gain.

IV. COMPARISON STUDY

To justify the superiority of the introduced topology, several key features of the proposed topology with other recent converters are compared and presented in Table II.

Related voltage gains of the converters introduced in Table II under the same conditions n_{21} = 0.65, n_{31} = 2.35 (three-winding CI-based), n = 3 (two-winding CI-based) are plotted over a wide range of the duty cycle in Fig. 10. It appears that the proposed converter offers higher DC Voltage gains than the compared topologies. As a result, the presented topology is able to provide high voltage gains under a low rate of turns ratios. Also, Fig. 11 depicts the voltage gain per number of components (M/N). From this figure, just the introduced circuit in this paper, and the converter in [26], have a higher M/N ratio at 0<D<0.6. The normalized voltage across the main power switch comparisons of the converters mentioned in Table *II* is shown in Fig. 12. It can be seen that the proposed topology has the lowest maximum voltage stress on the switch for all ranges of the duty cycle. Similarly, the normalized maximum voltage stress across the converter diodes in Table *II* is illustrated in Fig. 13. It can be seen that the voltage stress of the switching components of the suggested topology is at a reasonable level. Following what has been mentioned above in this section, the introduced converter possesses a low switch and diode voltage stresses. Therefore, MOSFET and diodes with lower-rated voltages can be chosen for the proposed circuit, which leads to efficiency improvement. Notably that the smaller turns ratio of the proposed circuit decreases the parasitic components of the windings of the coupled-inductor and reduces the core and copper losses.

Moreover, a comparison of the theoretical efficiency under the same conditions (*25V/400 V, 400 W, 60 kHz, n_{21} = 0.625, n_{31} = 0.875* and $n = n_{21}+n_{31}=1.5$ is provided in Table III. The parasitic components are chosen based on related datasheets. Because of full soft-switching performance along with very low reverse recovery loss, the proposed topology demonstrates the highest efficiency against others.

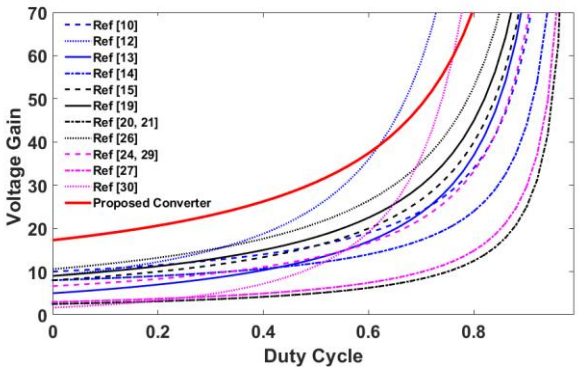


Fig. 10. Voltage gain comparison with other converters.

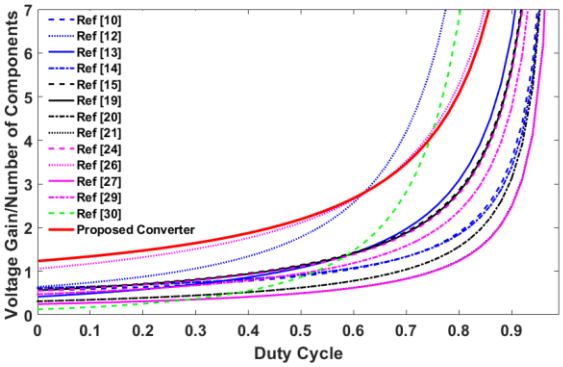


Fig. 11. The voltage gain per number of components comparison.

TABLE II. COMPARISON OF THE PROPOSED CONVERTER AND OTHER CONVERTERS.

Converter Topology	No. of Components S/D/C/CI+L/T	Voltage Gain	L.I.C.R	Voltage Stress on Main Switch	Maximum Voltage Stress on Diodes	Soft-Switching (Main Switch)	Reverse Recovery Loss
[10]	1/8/8/1^{2w}+0/18	$\frac{4+n(2-D)-D}{(1-D)}$	No	$\frac{V_o}{4+n(2-D)-D}$	$\frac{(n(2-D)-D)V_o}{4+n(2-D)-D}$	-	High
[12]	2/5/5/1^{2w} +1/14	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	No	$\frac{(1-D)V_o}{3+2n-(3+n-D)}$	$\frac{n(2-D)V_o}{3+2n-(3+n-D)}$	ZCS	Very Low
[13]	1/4/5/1^{2w} +1/12	$\frac{2+n+nD}{(1-D)}$	Yes	$\frac{V_o}{2+n+nD}$	$\frac{(1+n)V_o}{2+n+nD}$	ZCS+QR	Very Low
[14]	2/4/5/1^{2w} +1/13	$\frac{2(1+D)+2n(1-D)}{(1-D)}$	Yes	$\frac{V_o}{2(1+D)+2n(1-D)}$	$\frac{(1+n)V_o}{2(1+D)+2n(1-D)}$	ZCS	Low
[15]	1/5/6/1^{2w} +1/14	$\frac{2(1+n)}{(1-D)}$	Yes	$\frac{V_o}{2(1+n)}$	$\frac{V_o}{2}$	ZCS	Low
[19]	2/6/6/1^{2W}+1/16	$\frac{2n+3}{(1-D)}$	Yes	$\frac{V_o}{2n+3}$	$\frac{(1+n)V_o}{2n+3}$	ZVT	Low
[20]	1/3/3/1$^{\mathbf{2W}}$ +0/8	$\frac{2n-1}{(n-1)(1-D)}$	No	$\frac{(n-1)V_o}{2n-1}$	$\frac{nV_o}{2n-1}$	ZCS	Low
[21]	2/2/4/1$^{\mathbf{3W}}$ +1/10	$\frac{2n-1}{(n-1)(1-D)}$	Yes	$\frac{(n-1)V_o}{2n-1}$	$\frac{nV_o}{2n-1}$	ZVS	Very Low
[24]	1/5/5/1$^{\mathbf{3W}}$+0/12	$\frac{3+2n_{21}+n_{31}}{(1-D)}$	No	$\frac{V_o}{3+2n_{21}+n_{31}}$	$\frac{(1+n_{21}+n_{31})V_o}{3+2n_{21}+n_{31}}$	ZCS	Low
[26]	1/3/4/1$^{\mathbf{3W}}$ +1/10	$\frac{2+n_{31}-n_{21}}{(1-n_{21})(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{2+n_{31}-n_{21}}$	$\frac{(1+n_{31})V_o}{2+n_{31}-n_{21}}$	ZCS	Low
[27]	1/4/5/1$^{\mathbf{3W}}$ +1/12	$\frac{1+2n_{31}-n_{21}}{(n_{31}-n_{21})(1-D)}$	Yes	$\frac{(n_{31}-n_{21})V_o}{1+2n_{31}-n_{21}}$	$\frac{1+n_{31}}{1+2n_{31}-n_{21}}V_o$	ZCS+QR	Very Low
[29]	1/5/6/1$^{\mathbf{3W}}$+1/14	$\frac{3+2n_{21}+n_{31}}{(1-D)}$	Yes	$\frac{V_o}{3+2n_{21}+n_{31}}$	$\frac{(1+n_{21}+n_{31})V_o}{3+2n_{21}+n_{31}}$	ZCS	Low
[30]	1/5/5/1^{3w} +1/13	$\frac{1+n_{21}+n_{31}D}{(1-D)^2}$	Yes	$\frac{V_o}{1+n_{21}+n_{31}D}$	$\frac{(1+n_{21})V_o}{1+n_{21}+n_{31}D}$	-	High
Proposed Converter	1/5/6/1$^{\mathbf{3W}}$ +1/14	$\frac{2+D+n_{31}(2-D)-n_{21}}{(1-n_{21})(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{2+D+n_{31}(2-D)-n_{21}}$	$\frac{(1+n_{31})V_o}{2+D+n_{31}(2-D)-n_{21}}$	ZCS+QR	Very Low

Notes: S: Switch, **D**: Diode, **C:** Capacitor, **CI:** Coupled-Inductor, **L:** Inductor, **T:** Total Device Count, **L.I.C.R:** Low Input Current Ripple

TABLE III. *THEORETICAL EFFICIENCY OF THE CONVERTERS.*

Converter	[10]	[12]	[13]	[14]	[15]	[19]	[20]	[21]	[24]	[26]	[27]	[29]	[30]	Proposed Converter
Duty Cycle	0.77	0.51	0.74	0.73	0.65	0.66	0.72	0.8	0.7	0.66	0.51	0.69	0.67	0.5
Efficiency %	*95.2*	*90.7*	*95*	*94.8*	*95.0*	*92.7*	*89*	*94.9*	*95.1*	*94.2*	*93.2*	*94.8*	*91.4*	*95.1*

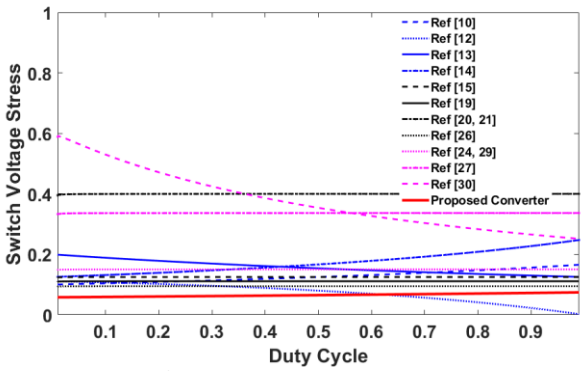


Fig. 12. Comparison of normalized voltage stress across the power switch of the converters given in Table *II* .

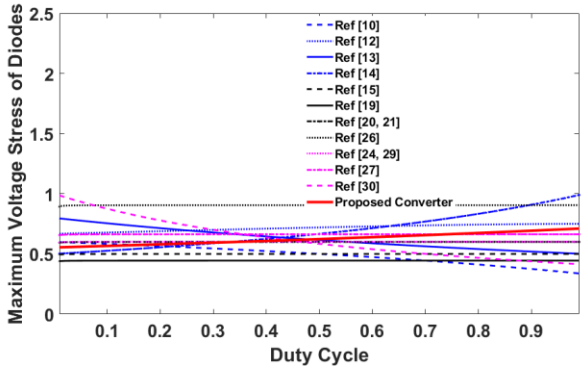


Fig. 13. Comparison of normalized maximum voltage stress of the diodes of the converters in Table *II* .

V. DCM PERFORMANCE ANALYSIS

A. *Boundary Between CCM and DCM*

In the proposed converter, the boundary condition between CCM and DCM performances occurs when the voltage across the magnetizing inductor reaches zero (V_{LM}=*0*), in which case the current of the diode D_1 falls to zero at t=t_8. Fig. 14 shows the voltage and current waveforms of the magnetizing inductor and the diode D_1 under in boundary operation. With the help of converter operation modes, the slope of increasing (m_1) and decreasing (m_2) the magnetizing inductor current is obtained as follows:

$$m_1 = \frac{V_{Cc}-V_{C1}}{L_{mB}(1-n_2)} = \frac{V_{in}}{L_{mB}(1-n_2)} \quad (42)$$

$$m_2 = \frac{-DV_{in}}{L_{mB}(1-n_2)(1-D)} \quad (43)$$

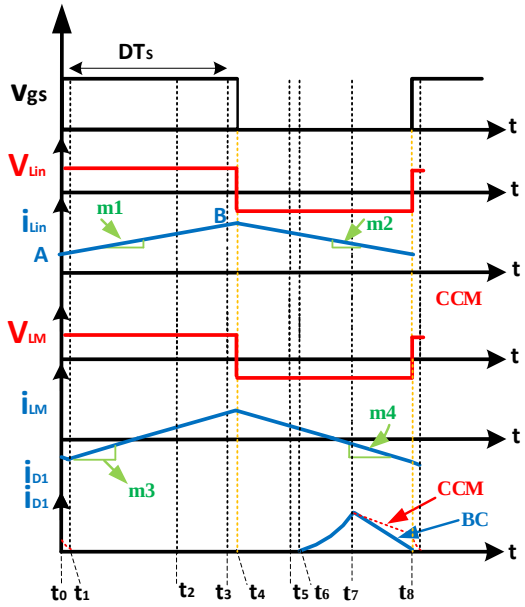


Fig. 14. The voltage and current waveforms of the L_m at the boundary of CCM and DCM mode. (*BC*=Boundary Condition).

$$m_3 = \frac{V_{Cc}-V_{C1}}{L_{mB}(1-n_2)} = \frac{V_{in}}{L_{mB}(1-n_2)} \quad (44)$$

$$m_4 = \frac{-DV_{in}}{L_{mB}(1-n_2)(1-D)} \quad (45)$$

According to the linear form of the charge and discharge of the input inductor current A and B in Fig.14 can be obtained as:

$$A = \frac{2M_{CCM}.I_o.L_{in}-DV_{in}T_S}{2L_{in}} \quad (46)$$

$$B = \frac{2M_{CCM}.I_o.L_{in}+DV_{in}T_S}{2L_{in}} \quad (47)$$

Given the average amount of magnetizing inductor current, and using (44) and (45), the boundary condition of the magnetizing inductance is derived as:

$$L_{M(min)} = \frac{2DL_{in}v_{in}}{2(1-n_2)f_s[2(1-n_3)I_oL_{in}+(1-n_2)\left(2M_{CCM}.I_o.L_{in}-DV_{in}\frac{1}{f_s}\right)]} \quad (48)$$

Regarding (48), the input DC voltage source, input inductor, output current, switching frequency and also the turns ratios of the TWCI affect the boundary condition value of the L_M. Furthermore, the normalized value of the boundary load resistance (R_{LB}) can also be given as:

$$\frac{R_{LB}}{L_{in}L_Mf_s} = \frac{2M_{CCM}^2.(1-n_2)^2+2M_{CCM}(1-n_3)}{DL_{in}+D(1-n_2)^2L_M} \quad (49)$$

Fig. 15 depicts the normalized value of the load resistance versus D and n at the boundary condition.

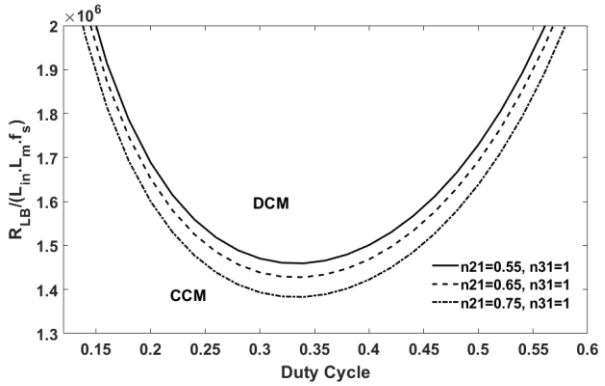


Fig. 15. Normalized the output load resistance versus D, n_{21} and n_{31}.

B. *Discontinuous Conduction Mode (DCM)*

Fig. 16 shows the voltage and current waveforms of the magnetizing inductor and the diode D_1 under DCM mode. In DCM operation, By applying the volt-second balance principle on L_{in} and L_M, the average voltages of C_c and C_1 are derived as follows:

$$V_{Cc} = \frac{1-\Delta}{1-D-\Delta}V_{in} \quad (50)$$

$$V_{C1} \approx \frac{D.V_{in}}{1-D-\Delta} \quad (51)$$

Which Δ represents the time duration $t_8<t<t_9$, which diode D_1 turns-off. Also, the voltage of the other capacitors are determined as:

$$V_{C2} = \frac{1-\Delta+n_{31}(1-D-\Delta)}{(1-n_{21})(1-D-\Delta)}.V_{in} \quad (52)$$

$$V_{C3} = \frac{n_{31}}{(1-n_{21})}.V_{in} \quad (53)$$

$$V_{Co1} = \frac{D+(1-\Delta)(1-n_{21})}{(1-n_{21})(1-D-\Delta)}.V_{in} \quad (54)$$

$$V_{Co2} = \frac{1-\Delta+n_{31}(2-D-\Delta)}{(1-n_{21})(1-D-\Delta)}.V_{in} \quad (55)$$

Eventually, the voltage gain of the proposed converter in DCM is derived as follow:

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{(1-\Delta)(2-n_{21})+D+n_{31}(2-D-\Delta)}{(1-n_{21})(1-D-\Delta)} \quad (56)$$

From (44) and (45), the time duration *1*-Δ as a function of converter parameters can be finded as:

$$1-\Delta = \frac{Q.M_{DCM}}{D}\left[(1-n_{31})+M_{DCM}(1-n_{21})-\frac{RD(1-n_{21})}{M_{DCM}L_{in}f_s}\right] \quad (59)$$

Which, Q is defined as :

$$Q = \frac{2L_Mf_s}{R}(1-n_{21}) \quad (60)$$

With substituting (50) into (47) and after rearranging, the voltage gain of the proposed converter at DCM condition can be calculated as a the third degree equation as:

$$aM_{DCM}^3 + bM_{DCM}^2 + cM_{DCM} + d = 0 \quad (61)$$

Which, *a*, *b*, *c*, and *d* are :

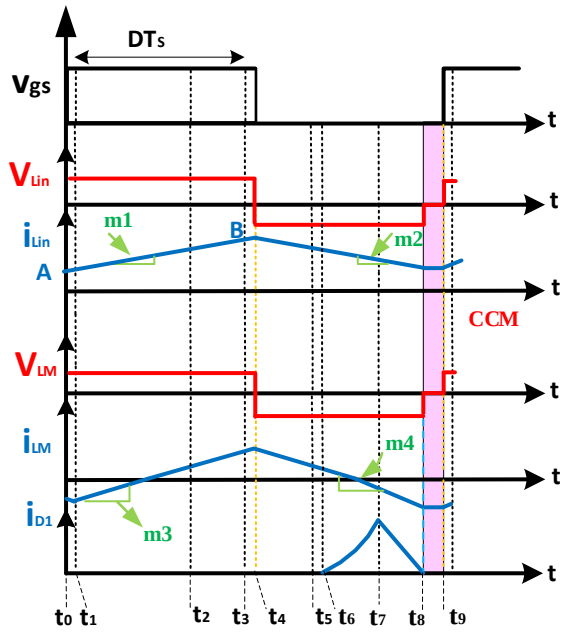


Fig. 16. The voltage and current waveforms of the L_m at DCM mode.

$$a = Q(1-n_{21})^2 \quad (62)$$

$$b = Q(-1+2n_{21}n_{31}+2n_{21}-2n_{31}-n_{21}^2) \quad (63)$$

$$c = -D^2(1-n_{21}) + Q(-2+n_{31}+n_{21}-n_{21}n_{31}+n_{31}^2) - DQQ_2(1-n_{21}) \quad (64)$$

$$d = -D^2 - Dn_{31}(1-D) - DQQ_2(2+n_{31}-n_{21}) \quad (65)$$

Which, Q_2 is defined as :

$$Q_2 = \frac{R(1-n_{21})}{L_{in}f_s} \quad (66)$$

VI. Design Considerations

A. Input Inductor

For RES (PV, FC, and battery), lower input current ripples are preferred. The minimum value of the input inductor L_{in} is selected to limit the input current ripple within the desired value as:

$$L_{in} > \frac{V_{in}.D}{\Delta I_{in}.f_s} \quad (67)$$

Here, ΔI_{in} is the permitted input current ripple.

B. Magnetizing Inductance Design

The proper value of the magnetizing inductor L_M of the TWCI can be designed by:

$$L_M > \frac{V_{Lm}.D}{\Delta I_{LM}.f_s} \quad (68)$$

It should be noted that selecting a very small current ripple for the magnetizing inductor of the TWCI (ΔI_{LM}) increases the wire consumption and the conduction losses.

As mentioned above, the voltage gain of the proposed converter can be regulated by three independent parameters D, n_{21}, and n_{31}. From Fig. 6, the acceptable range of duty cycle is about 0.4 <D< 0.65. Moreover, regarding (20) and Fig. 4, a slight increase of the second turns ratio n_{21} toward unit makes a significant increase in the voltage gain, which reduces the whole turns ratios and wire consumption. Nevertheless, choosing the turns ratio very close to unity is not recommended.

C. Capacitors

To suppress the output voltage ripple, the output filters' capacitance values $C_{o1,2}$ of this prototype can be determined as:

$$C_{o1} = \frac{DI_o}{\Delta V_{co1}.f_s} \quad (69)$$

$$C_{o2} = \frac{(1-D)I_o}{\Delta V_{co2}.f_s} \quad (70)$$

Here, $\Delta V_{Co1,2}$ are the tolerant output voltage ripple, which usually is selected as $\Delta V_{Co} \approx 1\%.V_o$. The middle capacitors of the converter are employed to transfer the input energy to the output. These capacitances can be calculated as follows:

$$C_c = \frac{D.i_{LK}}{\Delta V_{Cc}.f_s} = \frac{\pi(n_{21}+2n_{31})V_{out}}{\Delta V_{Cc}2R_L.(1-n_{21})f_s} \quad (71)$$

$$C_1 = \frac{D.i_{N2}}{\Delta V_{C1}.f_s} = \frac{\pi(1+2n_{31})V_{out}}{\Delta V_{C1}2R_L.(1-n_{21})f_s} \quad (72)$$

$$C_2 = \frac{i_{D2}.D}{\Delta V_{c2}.f_s} = \frac{\pi V_{out}}{\Delta V_{c2}.2R_L.f_s} \quad (73)$$

$$C_3 = \frac{i_{D3}.D}{\Delta V_{c3}.f_s} = \frac{\pi V_{out}}{\Delta V_{c3}.2R_L.f_s} \quad (74)$$

The capacitors C_c and $C_{1\text{-}3}$ do not perform filtering effect, So there is no need to design them based on very small voltage ripples. In this case, the converter's efficiency is also improved by selecting the film-type capacitors with lower parasitic resistance. Moreover, the simplest method to adjust the resonant frequency is by C_c and C_1 from (75) as:

$$\pi\sqrt{L_{k1}\left[\left(\frac{2n_{21}.n_{31}+1}{2n_{31}+1}C_1\right)\middle\|\, C_c\right]} = DT_S \quad (75)$$

VII. Experimental Verification

A 400W 25V-to-400V laboratory prototype that operates at 60 kHz switching frequency is built and tested to justify the correctness and effectiveness of the presented circuit. The components specifications of the sample prototype are summarized in Table *IV*. The low voltage stress across the power switch makes it possible to select a MOSFET IRFB4110 with 100 *V* voltage rating and low $R_{DS(on)}$. The measurement instruments PA-667 (1 *MHz* current probe) and *GDP- 025* (differential voltage probe) are used to obtained the current and voltage waveforms of the components. PA-667 has two division coefficients including, 500 mV/A and 50 mV/A, and *GDP-025* also has three different division coefficients including, *x20, x50*, and *x200*.

Fig. 17 demonstrates the steady voltage stress and current shapes of the single power switch. It is evident that the switch turns ON under ZCS conditions with voltage stress of about 52*V*. Moreover, the resonant performance in the operating Mode 2 decreases the value of the switch current at the turn-off instant. From Fig. 18 (a)-(d) and Fig. 19 (a), the current of all diodes of the proposed converter turns OFF at LRR conditions. Furthermore, the voltage stresses across the diodes are about V_{D1} *=120 V*, V_{D2} *=220 V*, V_{D3} *=100 V*, V_{Dc} *=52 V, and* V_{Do} *=220V*, which are more lower than the output voltage.

TABLE *IV*: SPECIFICATIONS AND COMPONENTS OF PROTOTYPE SETUP.

Parameter	Values
Output Power (P_{out})	400 W
Input Voltage (V_{in})	25 V
Output Voltage (V_{out})	400 V
Switching Frequency (f_s)	60 kHz
Capacitor C_1	15 µF
Capacitor C_c	4.7 µF
Capacitors C_2, C_3	6.8 µF
Capacitors C_{o1}, C_{o2}	47 µF/100 µF
MOSFET *S*	IRFB4110 / $R_{DS(on)}$=3.7 mΩ
Input Inductor L_{in}	63 µH / T184-52
Magnetizing Inductor of the CL (L_m)	200 µH
Turns Ratios of the TWCI *(N1:N2:N3)*	(16:10:13) / EE55/28/21
Diodes D_1, D_3	MUR415 ($V_{F\,(Max)}$=0.71 V)
Diodes D_2, D_o	MUR440 ($V_{F\,(Max)}$=1.05 V)
Diodes D_c	MBR20100($V_{F\,(Max)}$=0.75 V)

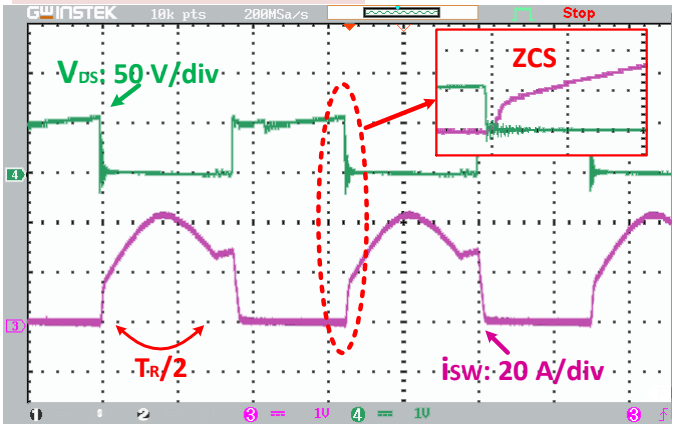
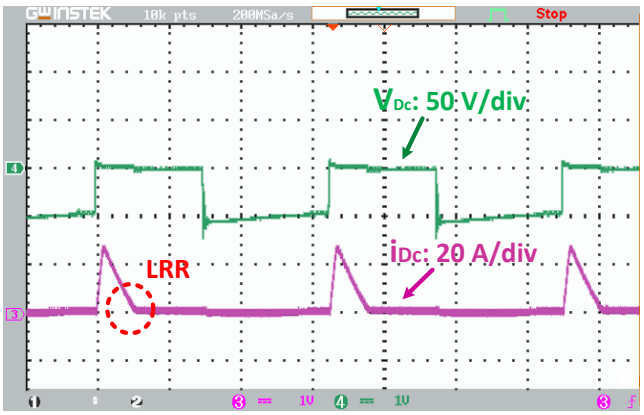
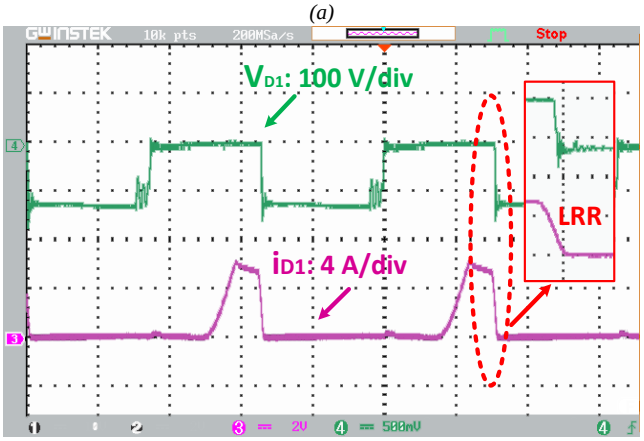


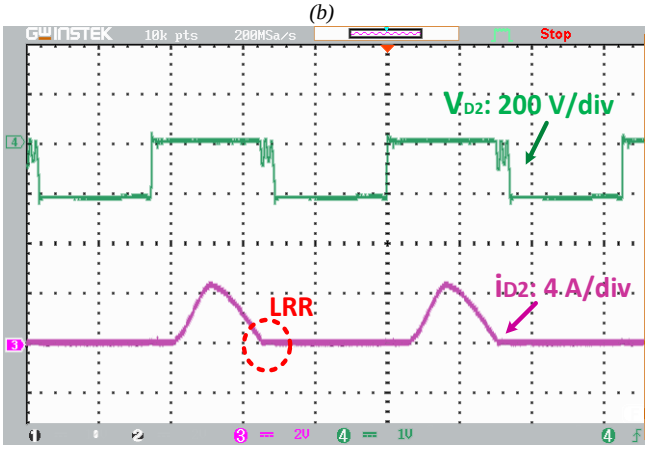
Fig. 17. The experimental waveforms of the Single Power MOSFET.



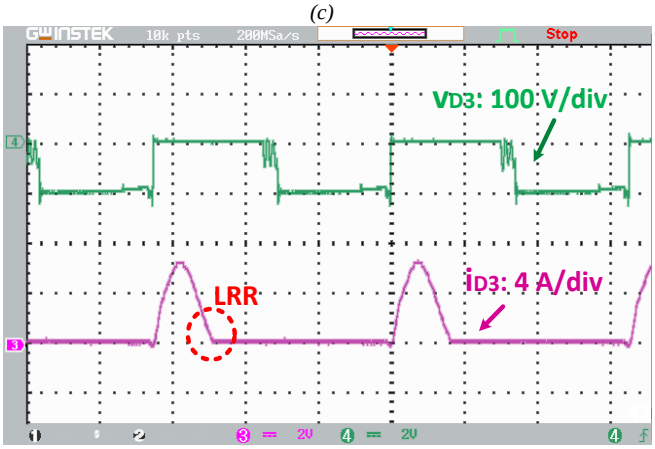
(a)



(b)



(c)

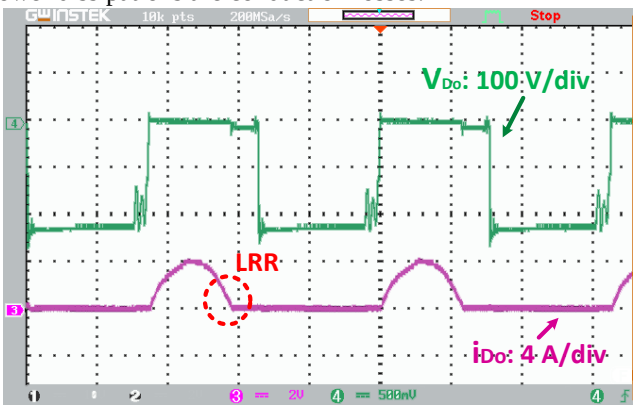


(d)

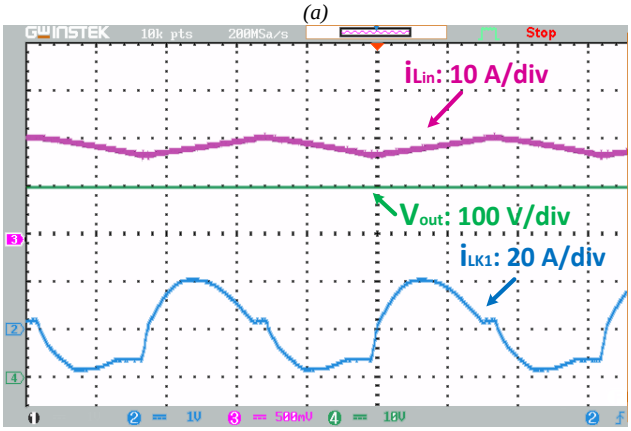
Fig. 18. The experimental waveforms.*(a) Diode D_c, (b) Diodes D_2 and D_3.*

Also, Fig. 19 (b) exhibits the experimental currents of the input and leakage inductors along with the output DC voltage. From this figure, the current ripples of the input inductor are very small and about 4 A. The full soft-switching performance makes the introduced topology offers the regulated DC voltage with at least voltage spike at the switching instants.

Fig. 20 represents the measured efficiency of the proposed circuit and the converters in [13], and [27] under full load condition(*25V/400V/400W*). Moreover, Fig. 21 (a)-(c) depicts the pie graphs of the theoretical power loss break-down at full load conditions of the mentioned converters against output power at full load conditions. In the converter [27], the capacitor power losses are significantly higher than the others. From these figures, the proposed converter has a more suitable performance. For the full load conditions (25 *V* - 400 *V*, 400*W*), the measured efficiency is about 93.5 %. Because of the soft-switching features for all switching devices, Less share of the power dissipations are conduction losses.



(a)



(b)

Fig. 19. The experimental waveforms.*(a) Diode D_o, and (b) V_o , i_{in} , and i_{LK1}.*

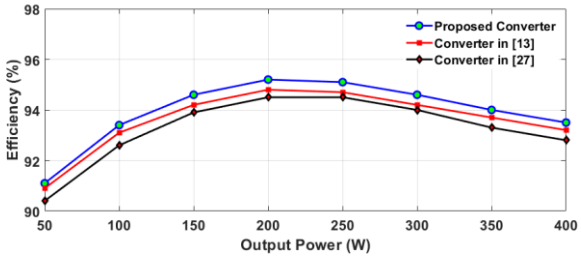


Fig. 20. Measured efficiency of the proposed converter and the converters in [13], and [27] under full load condition(25V/400V/400W).

Fig. 22 (a) - (b) presents the dynamic responses of the proposed topology under the output load and the input voltage variations, respectively. For this purpose, a closed loop controller (PI) is used. From this figure, when the output load changes from Po=400W (R_{Load1}=400 Ω) to Po=50W (R_{Load2}=3200 Ω), and the input voltage changes from V_{in1}=20 V to V_{in2}=25 V, the output DC voltage is regulated at 400V. In addition, the power loss distribution of the proposed circuit components is provided in Table *V*. The values of the parasitic resistances are measured with the help of a Hantek 1833C. Moreover, the actual values of the forward voltage drop of the diodes are obtained by their instantaneous currents. The experimental platform of the proposed converter is shown in Fig. 23.

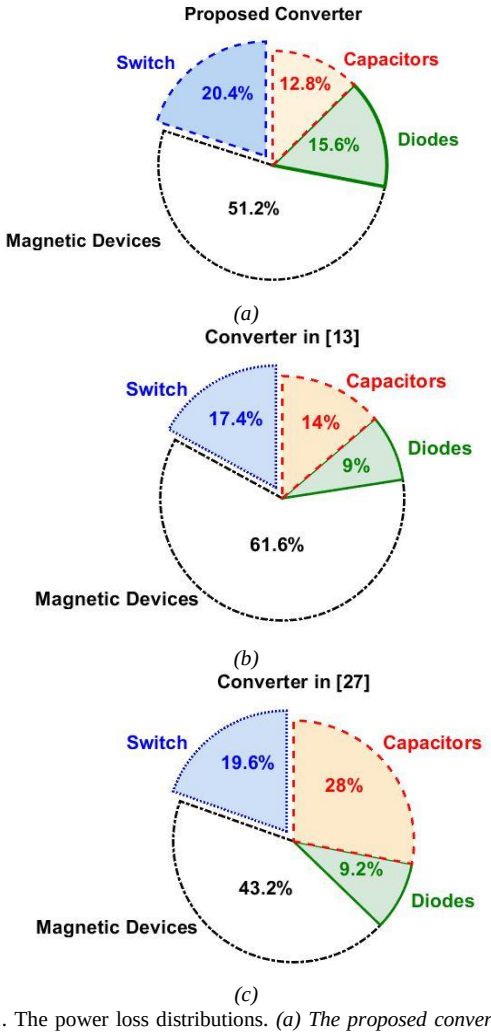
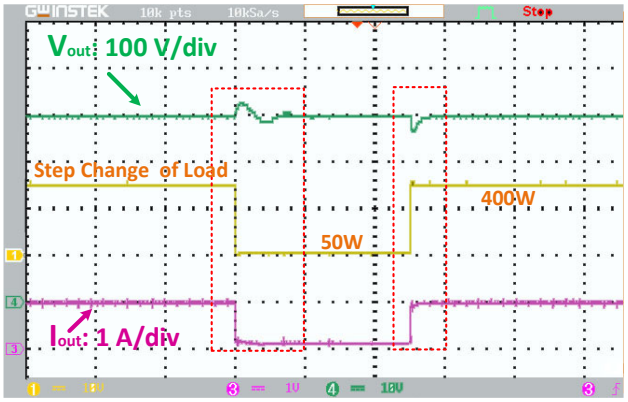
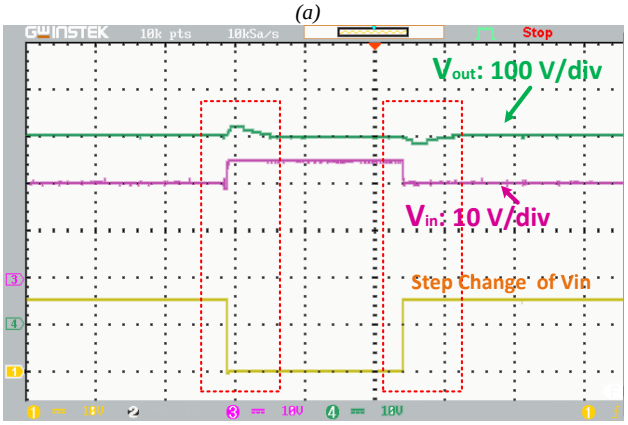


Fig. 21. The power loss distributions. *(a) The proposed converter, (b) Converter in [13], (c) Converter in [27] (25 V / 400 V/ 400 W).*



(a)



(b)

Fig. 22. Dynamic responses. (a) output Load from P_o=400 *W* to P_o=50*W*, (b) input voltage from V_{in}=20 *V* to V_{in}=25 *V*.

TABLE. V. *LOSS DISTRIBUTIONS OF THE PROPOSED TOPOLOGY.*

MOSFET Losses

Device	Type	P_{on} (W)	P_{off} (W)	$P_{con.}$(W)	$P_{Total.}$(W)
MOSFET	IRF4110	-	3.5	2	**5.2 W**

Diode Losses

Device	Type	V_F (V)	$P_{Di.}$ (W)
D_c	MBR20100	0.6	0.6
D_1	MUR415	0.7	0.7
D_2	MUR440	0.71	0.71
D_3	MUR420	0.7	0.7
D_o	MUR440	0.72	0.72
		Total	**3.43 W**

Capacitor Losses

Device	Type	ESR (mΩ)	$P_{Ci.}$ (W)
C_c	4.7 uF 100 V (MPX)	7.1	1.4
C_1	15 uF 100 V (MKS)	7	1.8
C_2	3.3 uF 100 V (MKS)	10	0.06
C_3	3.3 uF 160 V (MKS)	10	0.08
C_{o1}	47 uF 200 V	70	0.67
C_{o2}	100 uF 400 V	100	0.2
		Total	**4.2 W**

Magnetic Losses

Device	Type	$P_{Con.}$ (W)	$P_{Core.}$ (W)
L_{in}	T184-52	2.9	1.7
TWCI	EE42/21/20	9.1	0.11

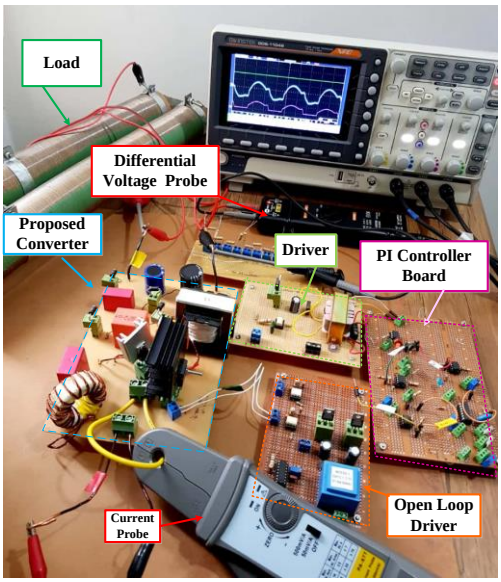


Fig. 23. The experimental platform and prototype.

VIII. Conclusion

A novel high voltage gain DC-DC converter is proposed and analyzed in this paper for high step-up applications. In the structure of the proposed circuit, a TWCI with VMC is combined to meet a high voltage conversion ratio. A regenerative passive clamp circuit is utilized to limit the steady voltage stress across the main power switch. Also, to better design the converter to gain the desired performance, there are three degrees of freedom (n_{21}, n_{31}, and D). Unlike most CI-based converters, because of the partial Transe-inverse features in the presented circuit, an ultra-high DC output voltage can be obtained under lower turn ratios of the TWCI. The presented structure has a significantly higher voltage gain and lower switch voltage stress over similar high gain topologies regarding the comparison section. Overall, the contributions of the proposed converter include ultra-high voltage conversion ratio under full soft-switching performance, continuous input current with low ripple, low voltage stress, common ground, and decent efficiency. Finally, the experimental results from a 200 W, 30 V-250 V laboratory prototype have verified the effectiveness of the introduced DC-DC topology.

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